

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**



FIG. 1

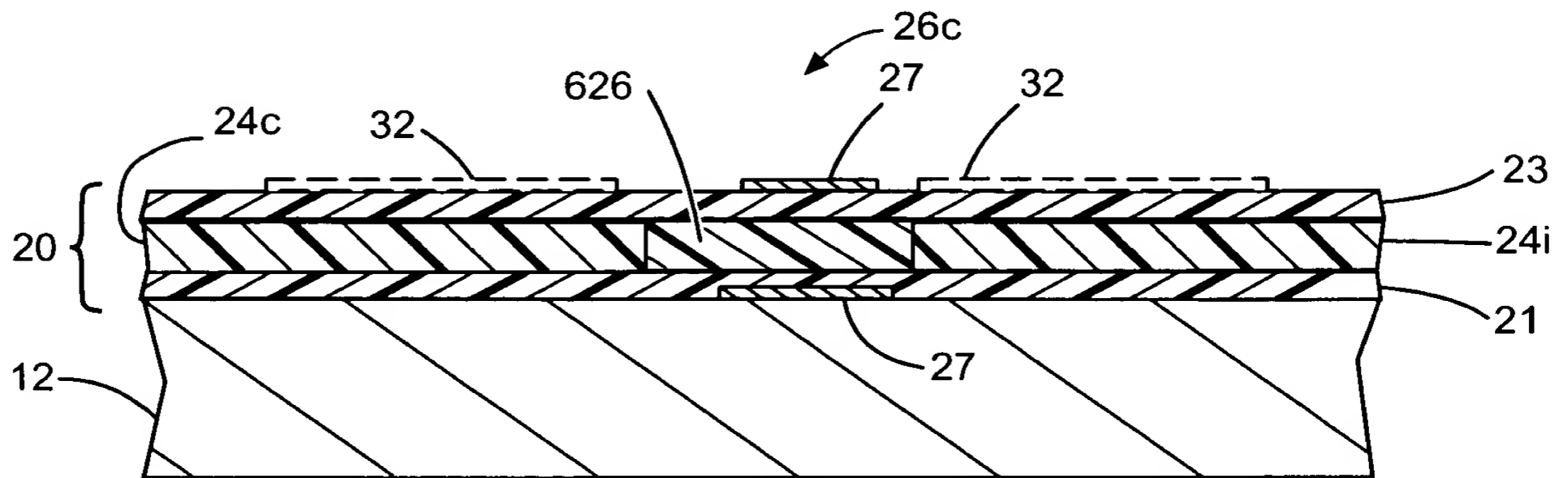


FIG. 2

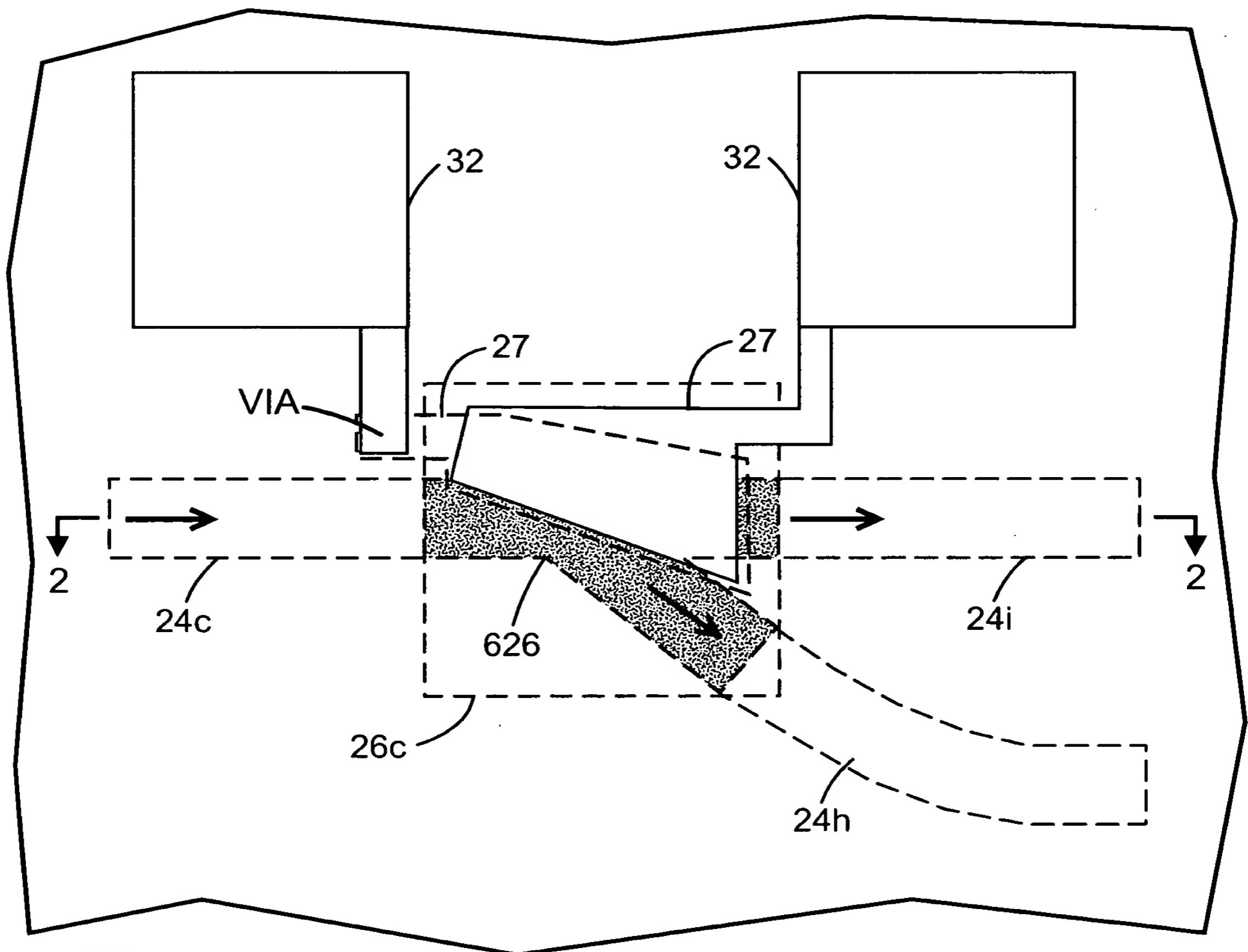


FIG. 3

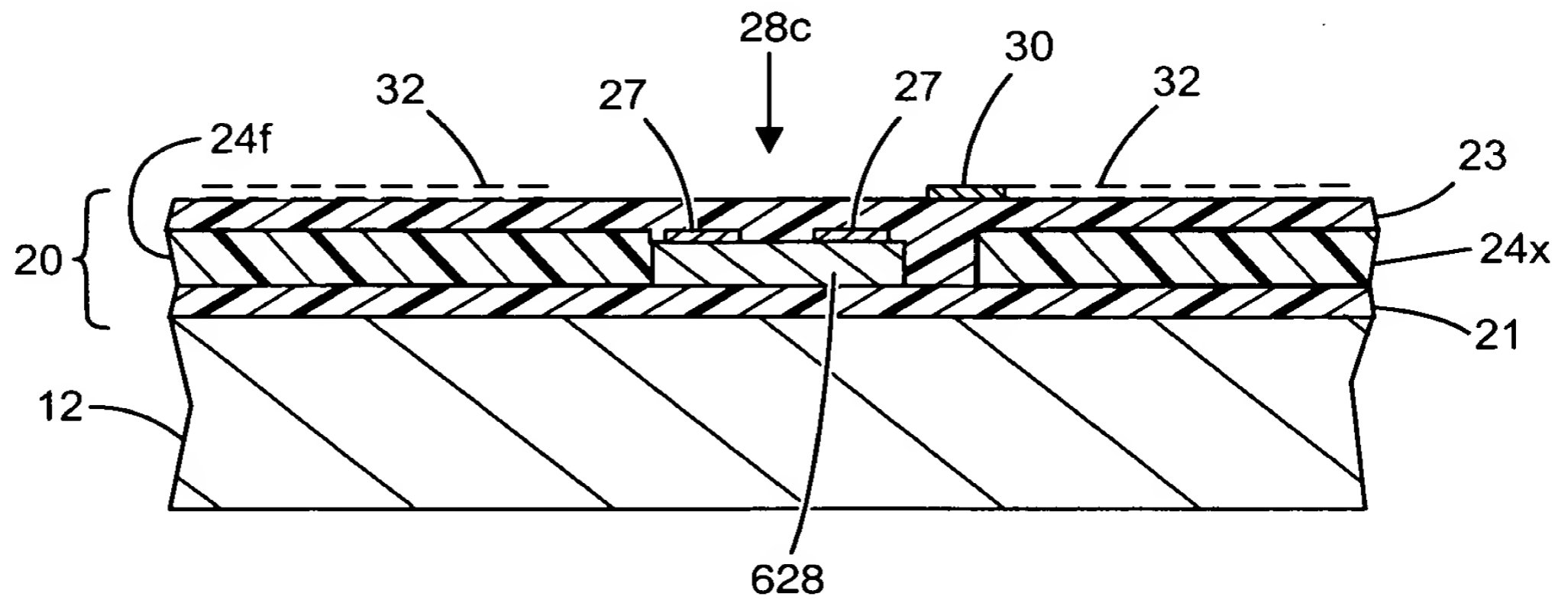


FIG._4-1

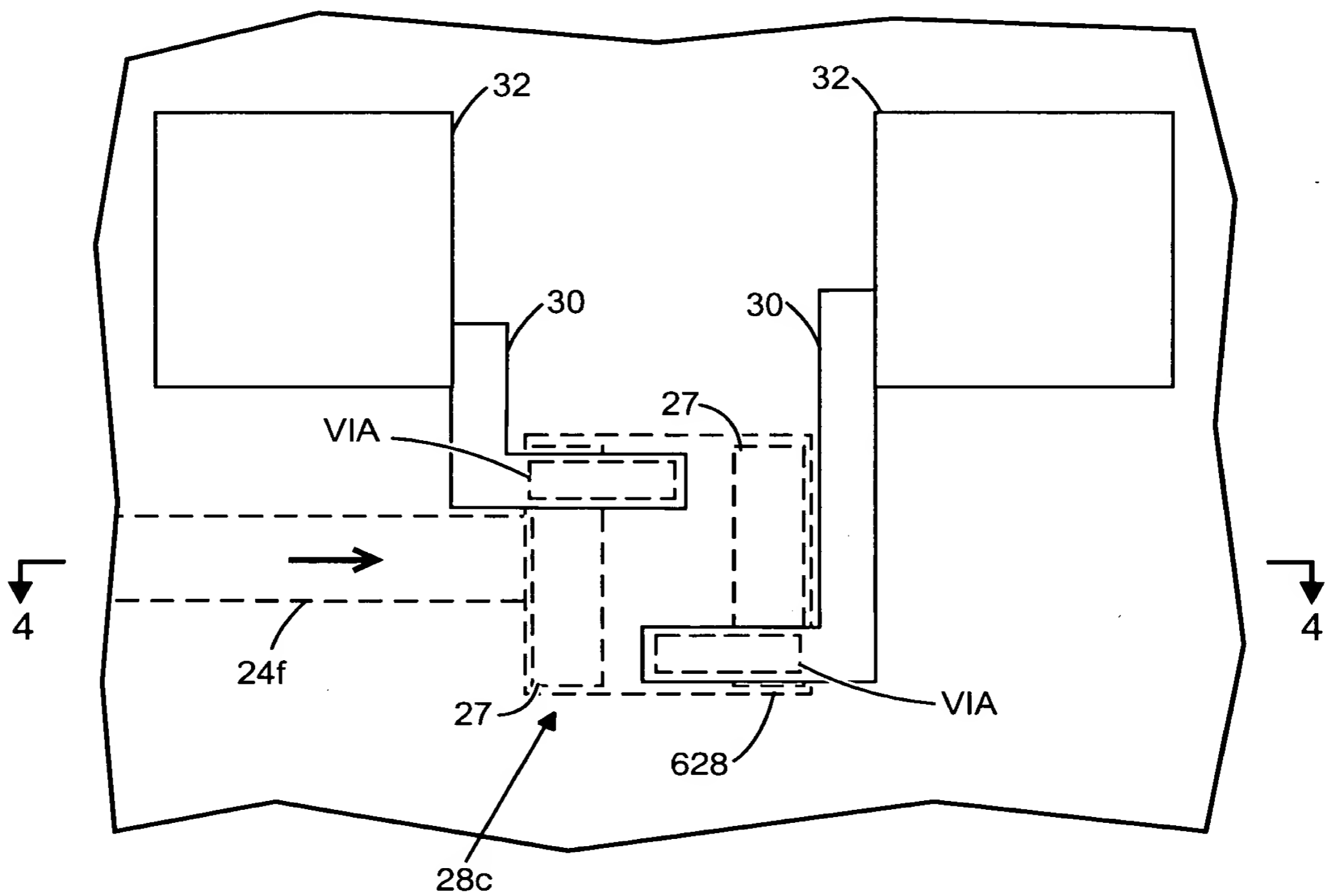


FIG._5-1

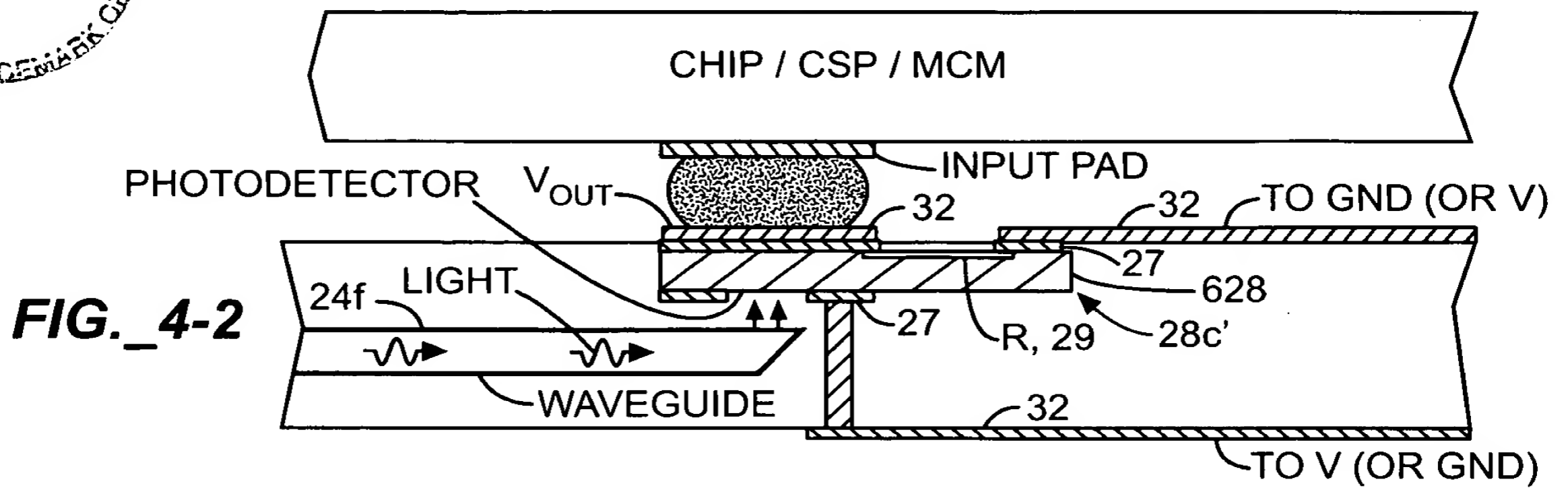


FIG. 4-2

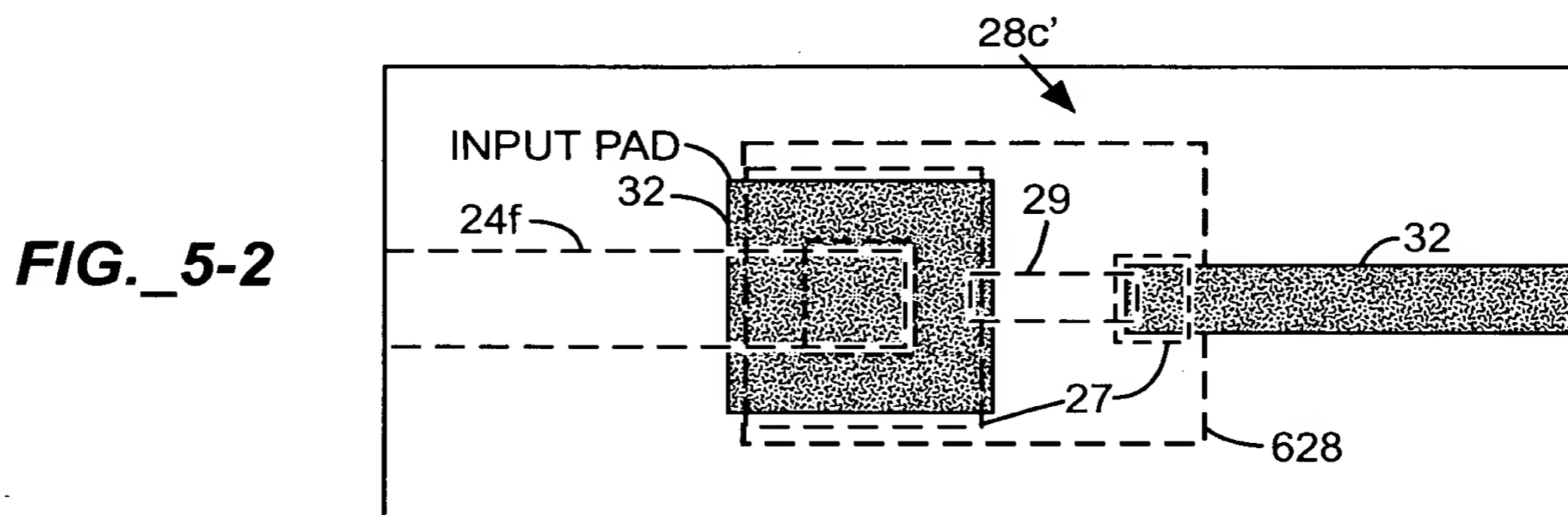


FIG. 5-2

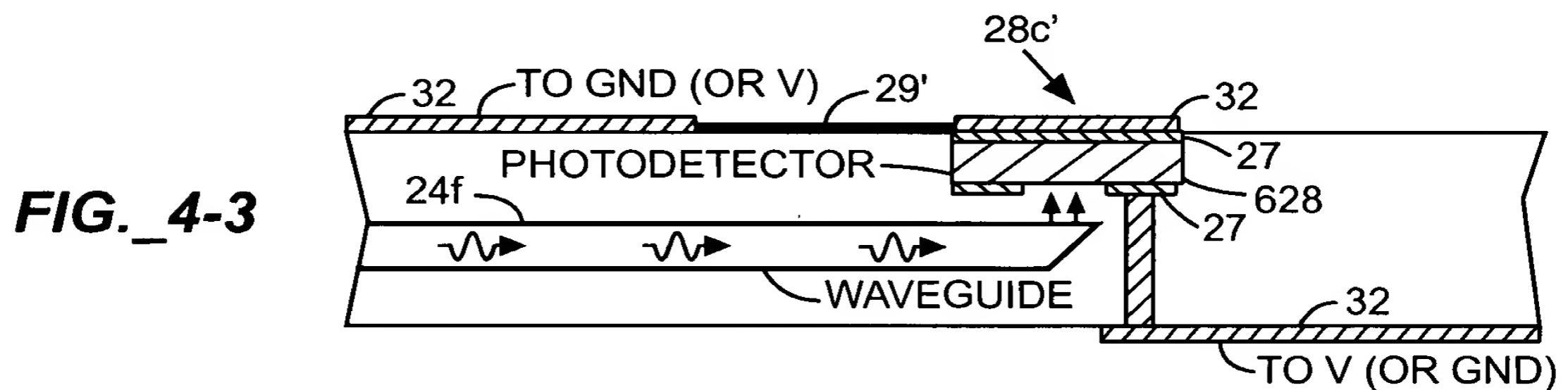


FIG. 4-3

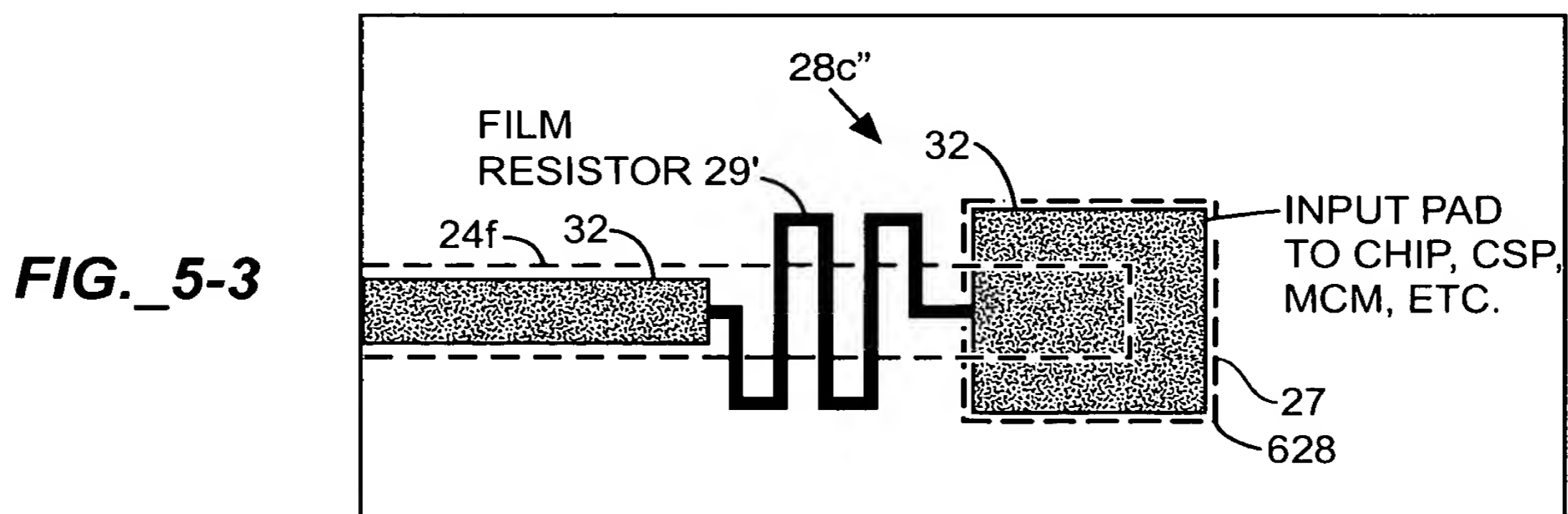


FIG. 5-3



FIG. 6



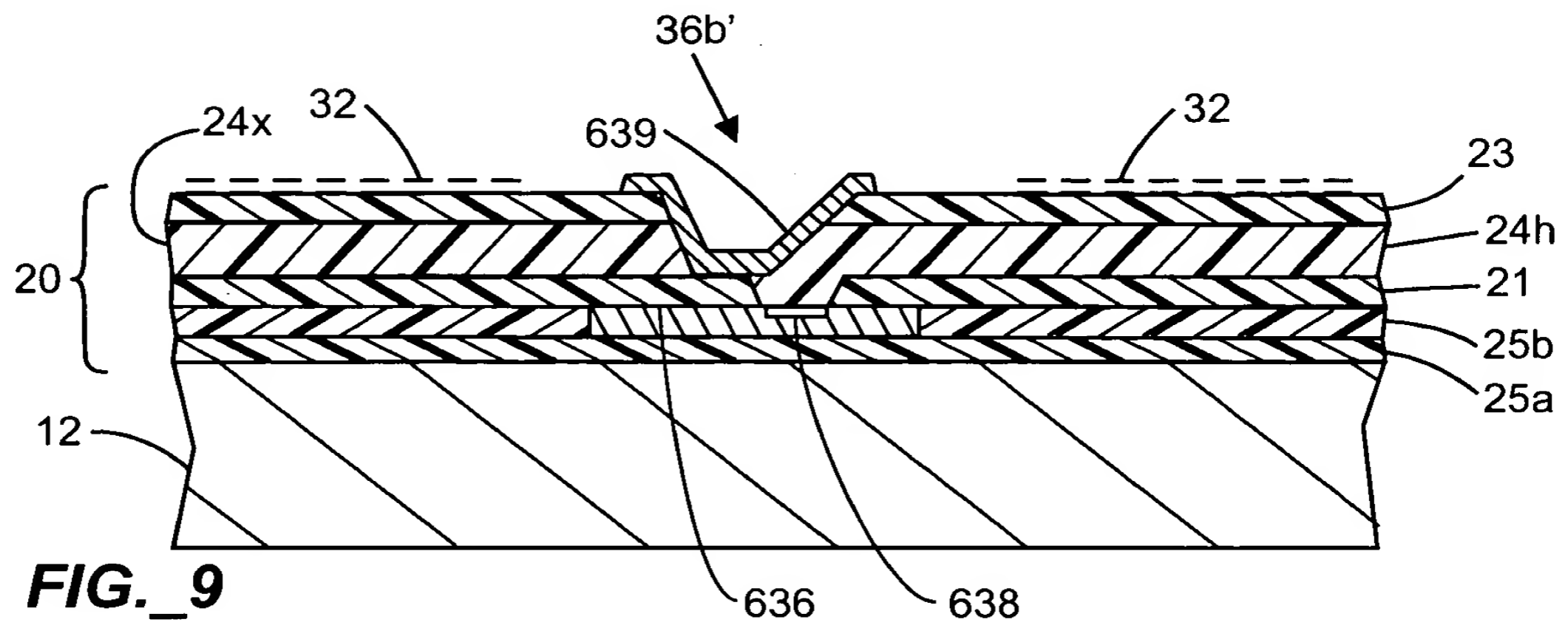


FIG. 9

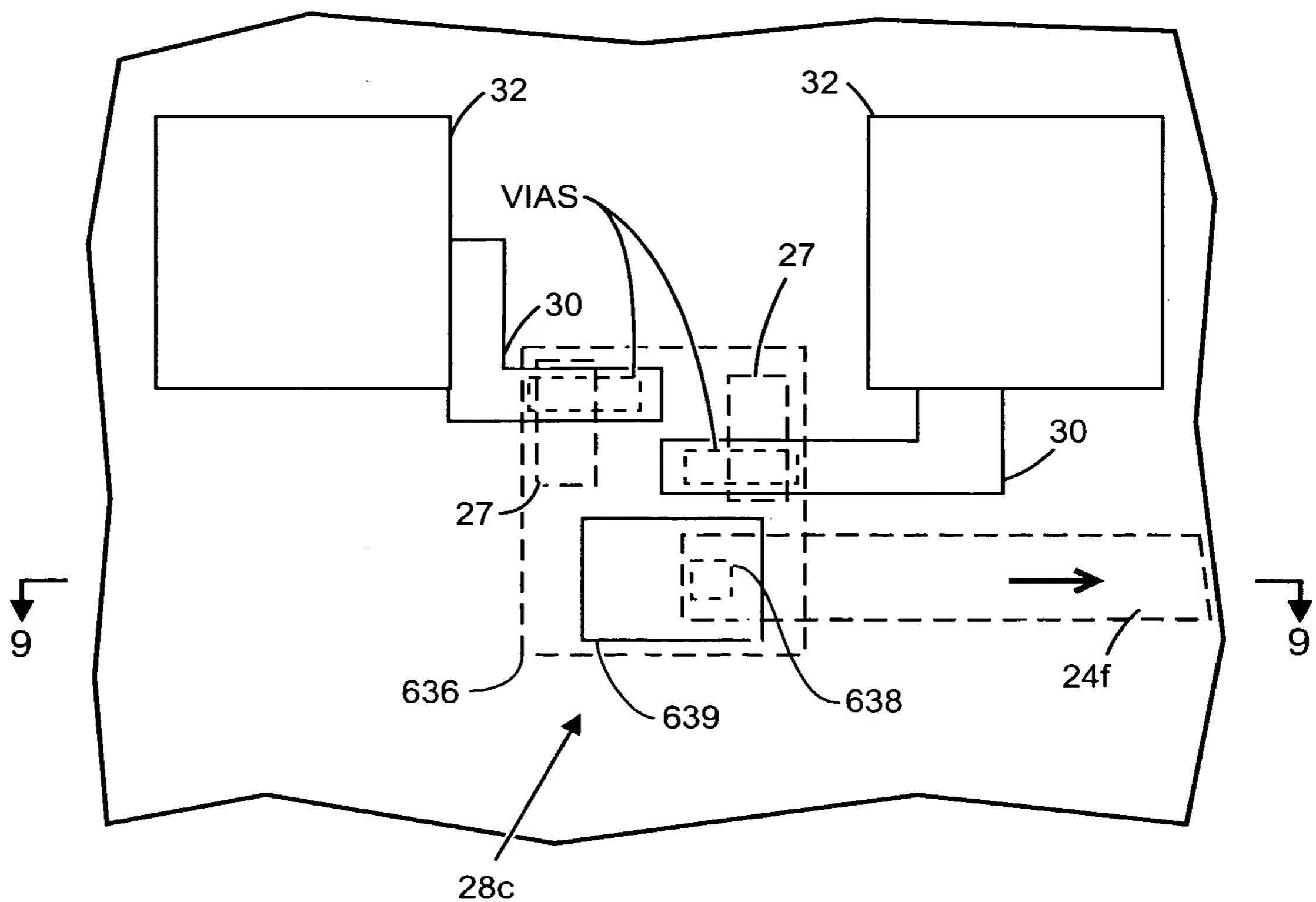
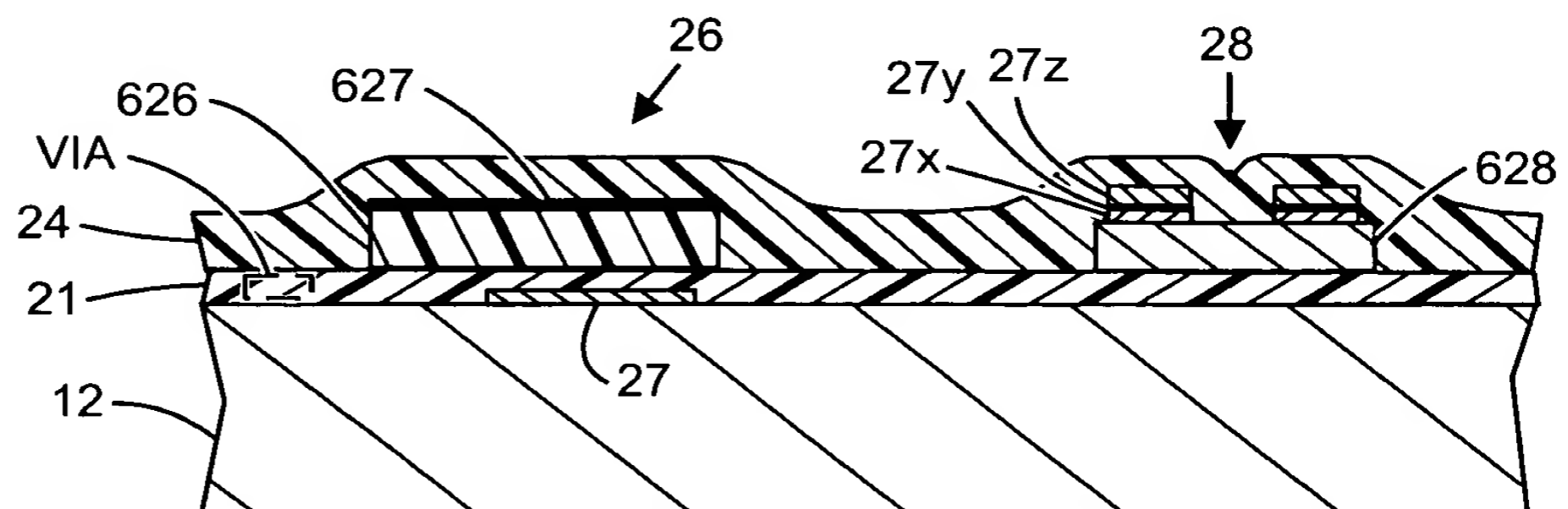
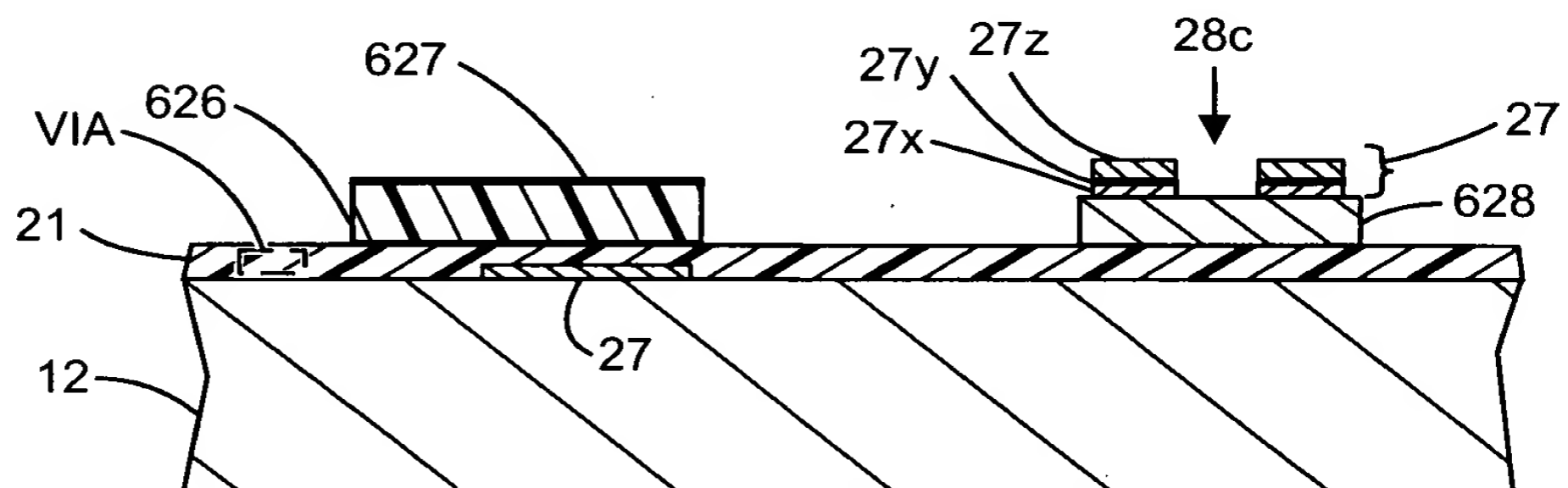
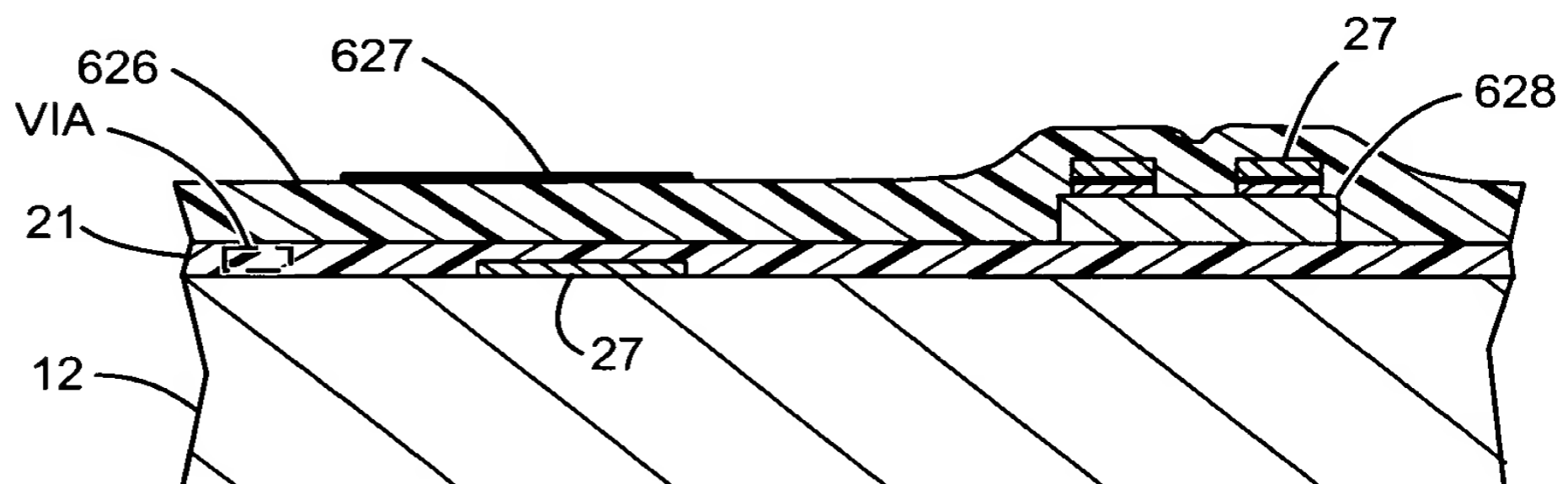
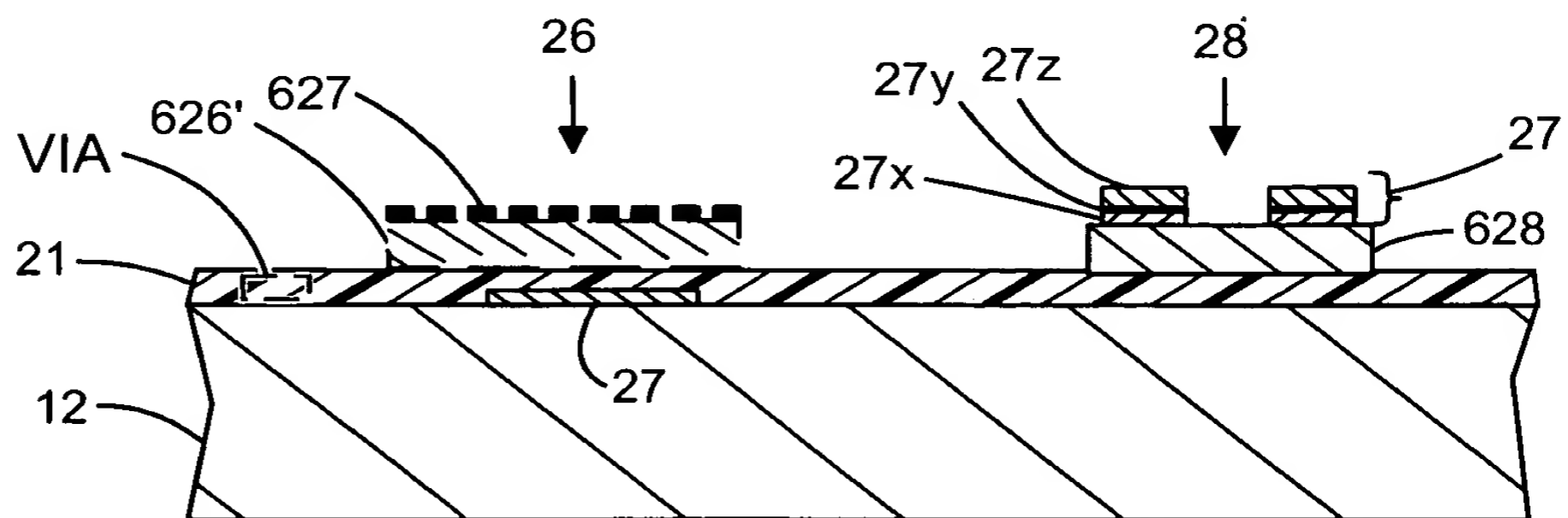


FIG. 10





9 / 61

FIG._15

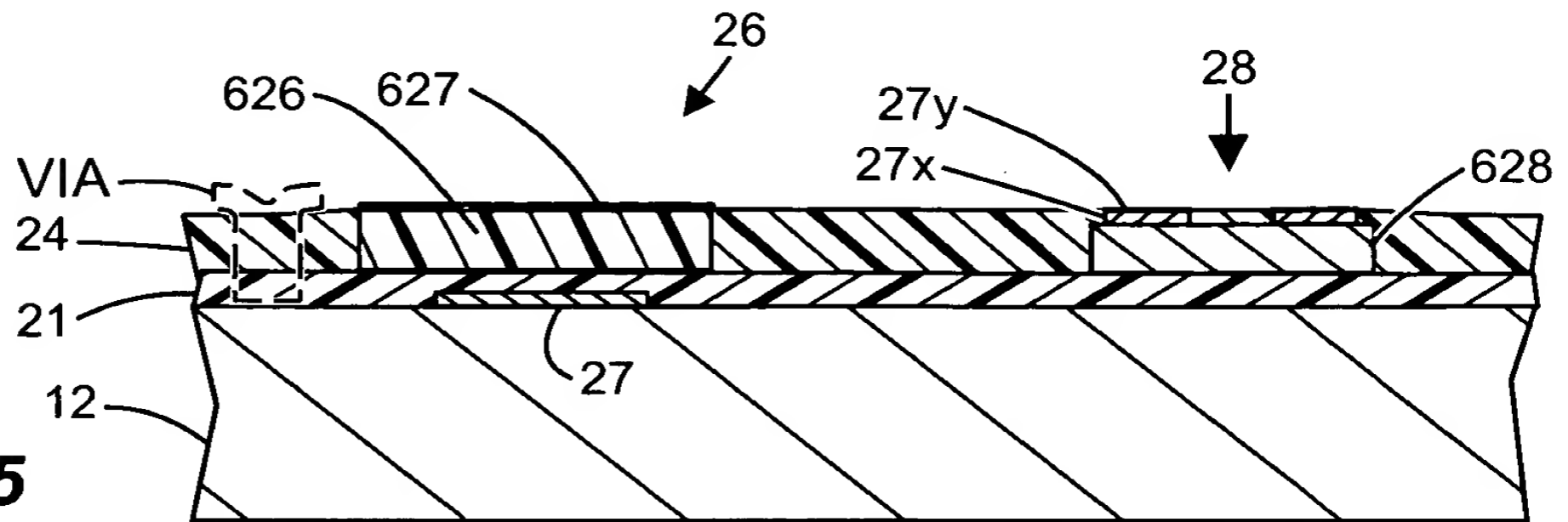


FIG._16

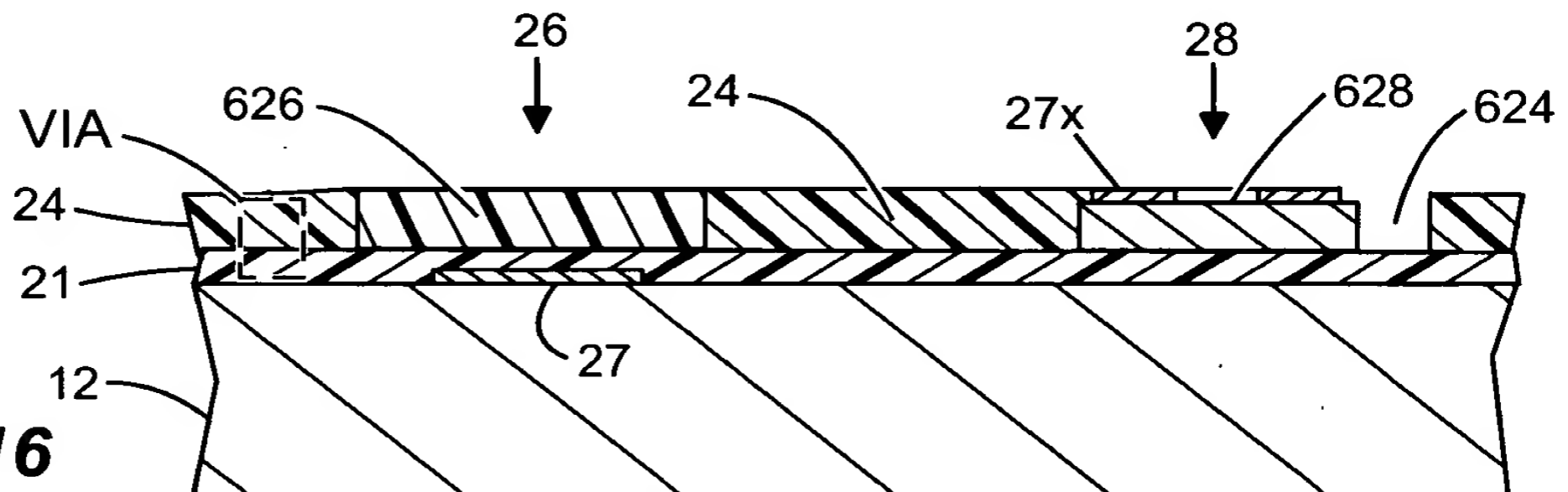


FIG._17

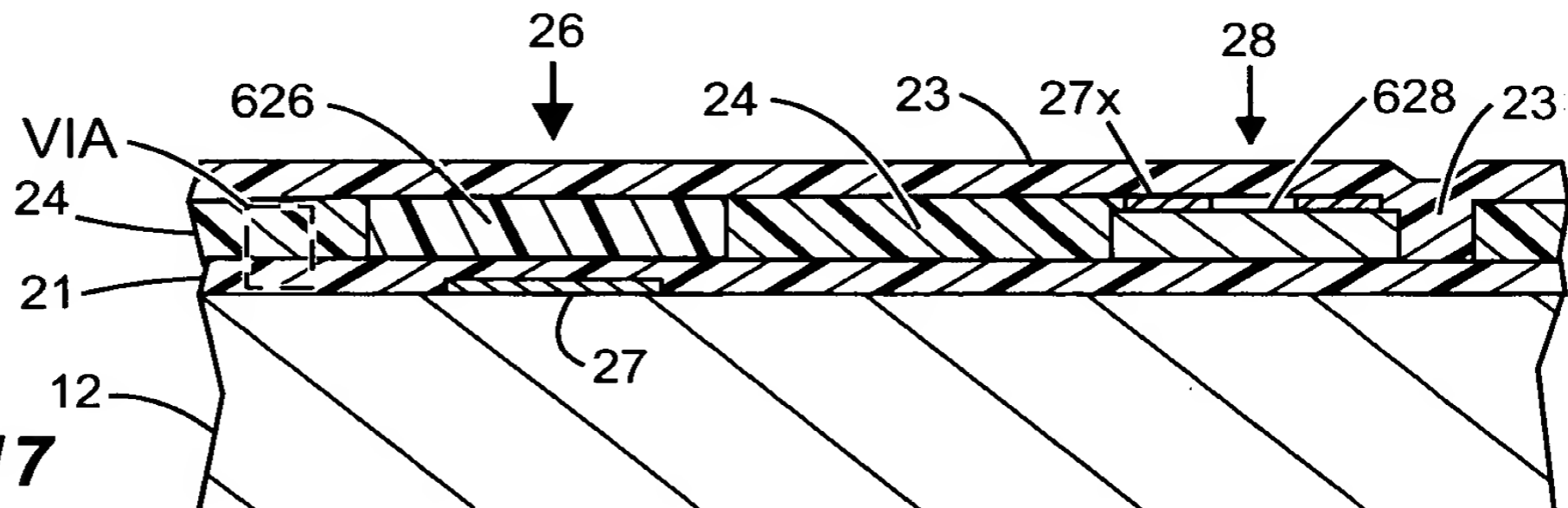
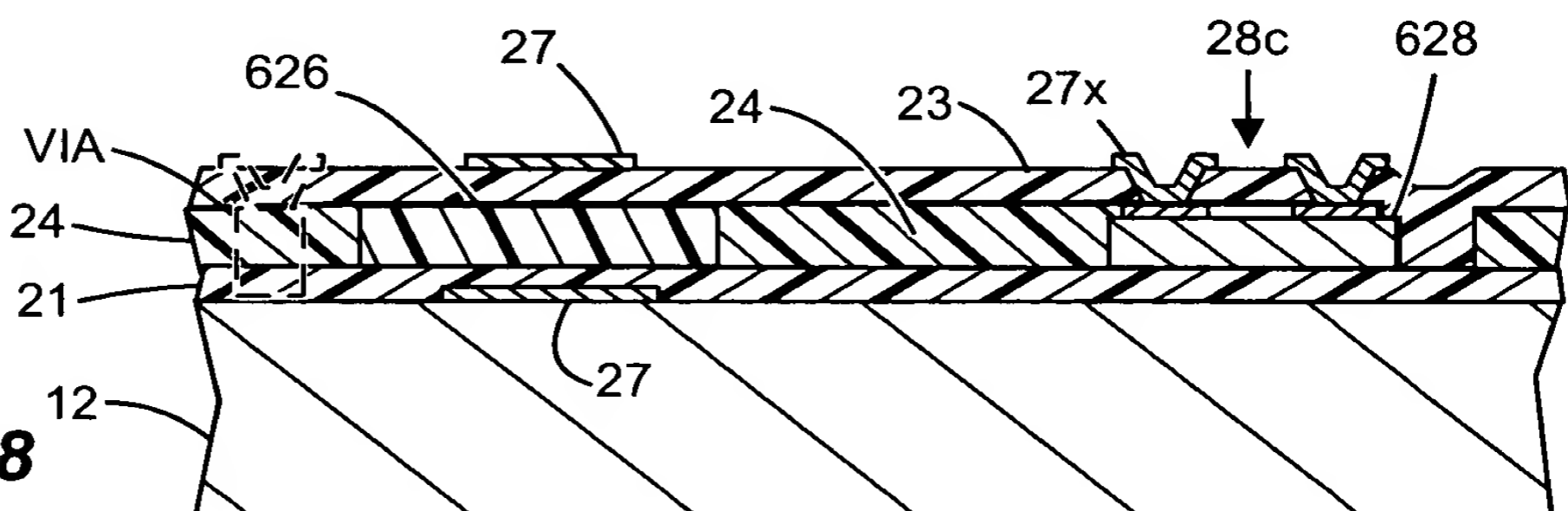


FIG._18



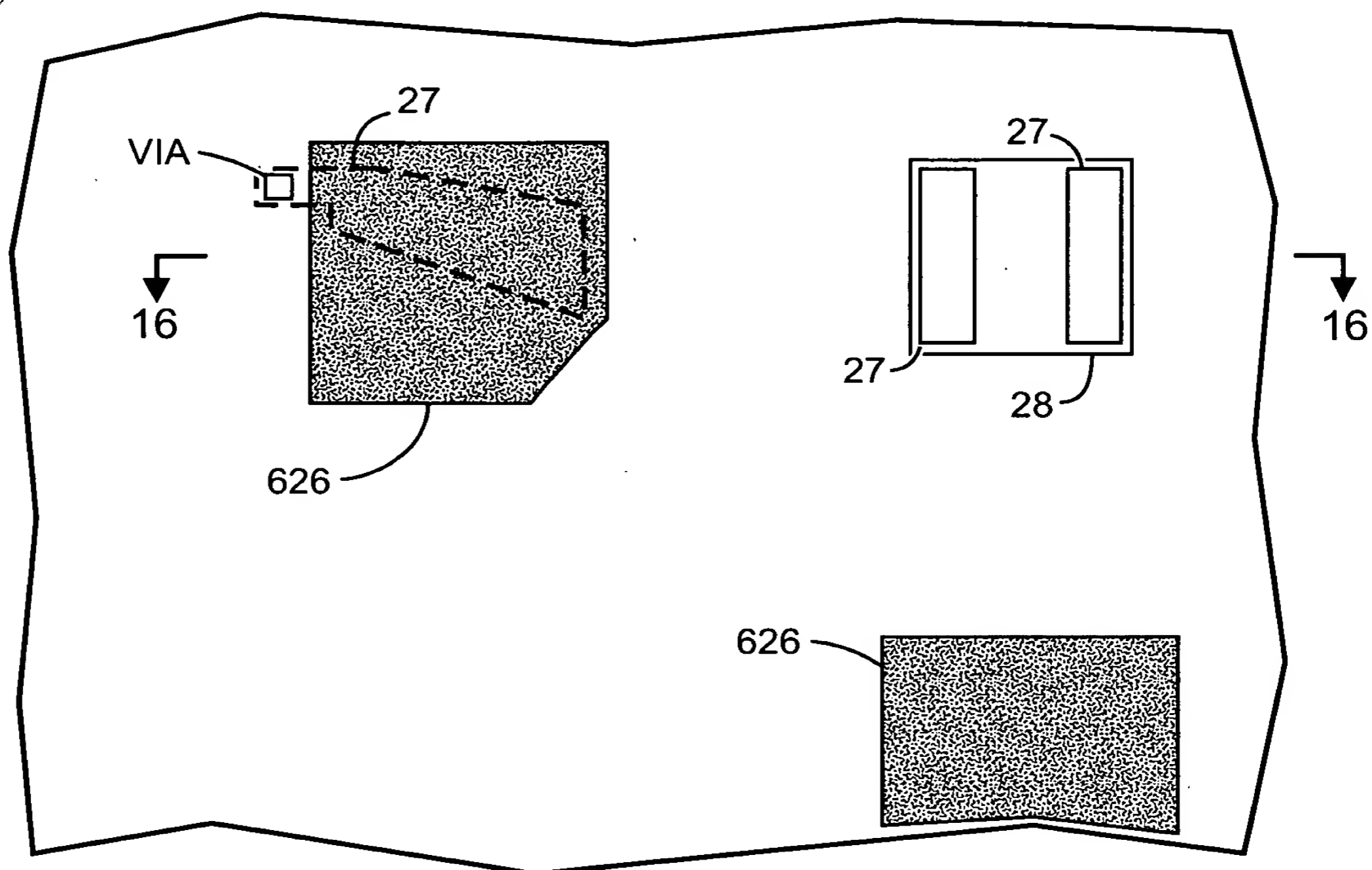
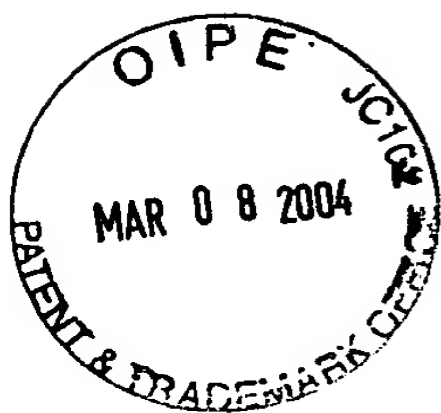


FIG._19

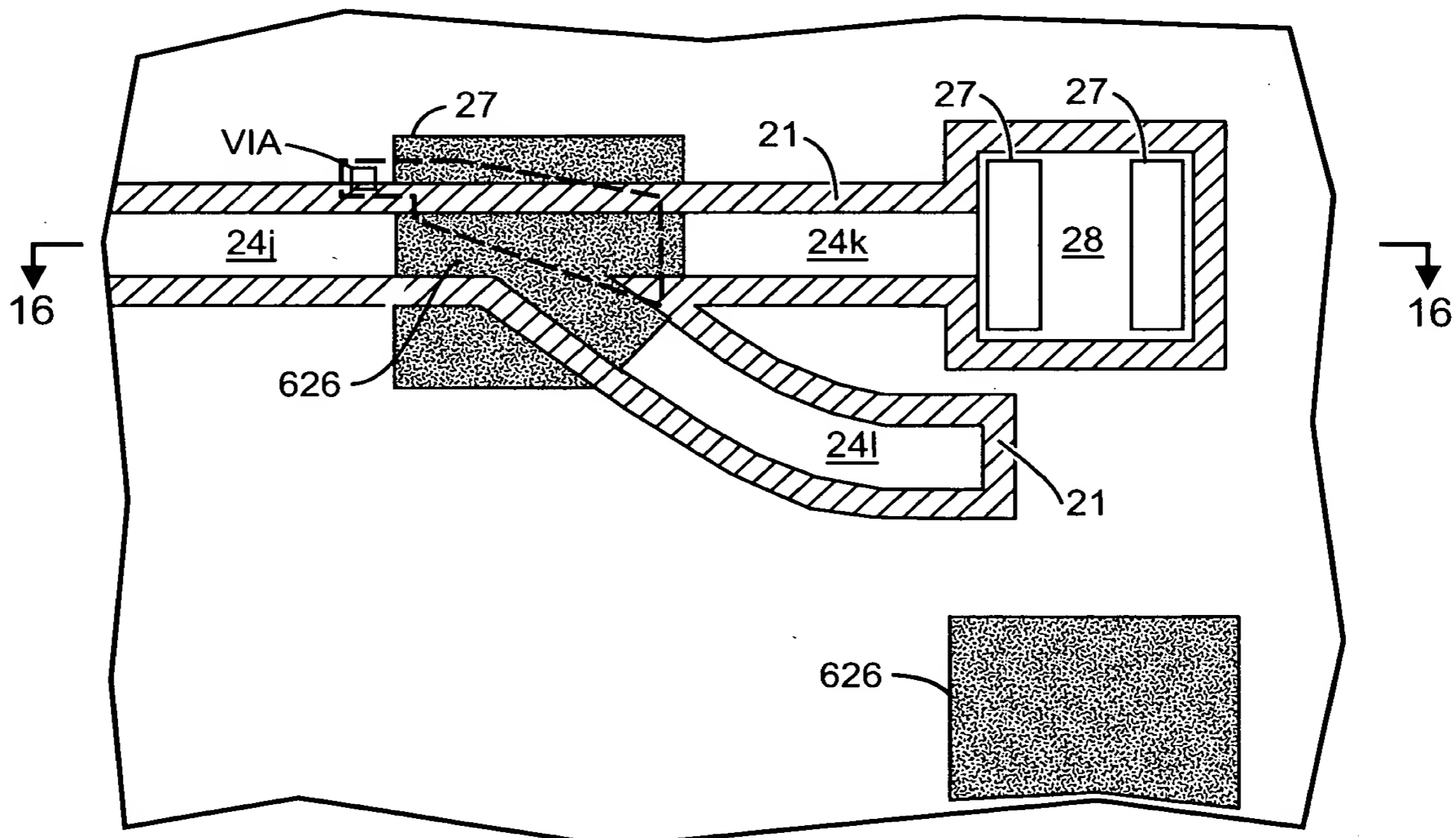


FIG._20

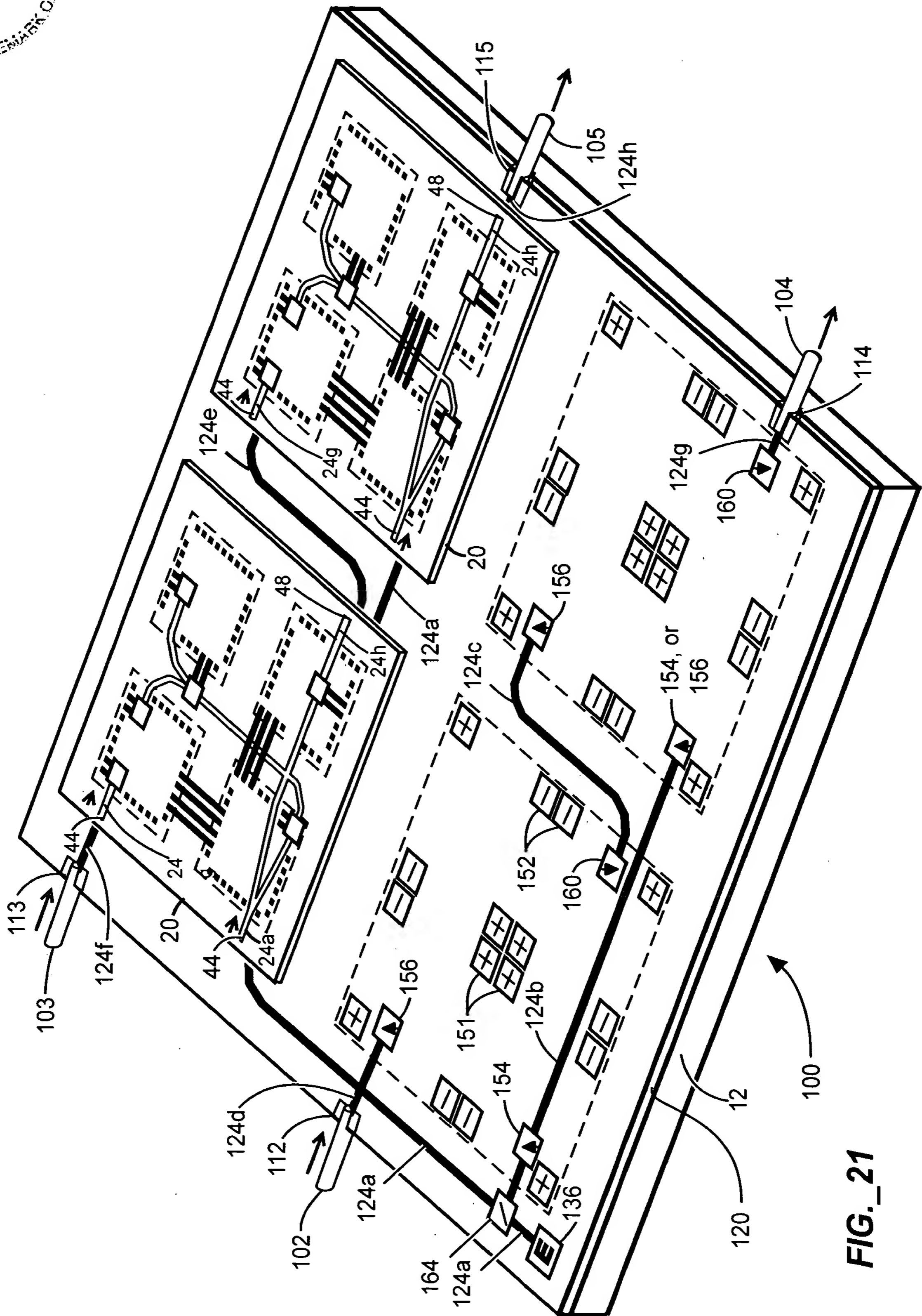


FIG. 21

Inventors: Tetsuzo Yoshimura, et al.
Application Serial No.: 09/295,431

12 / 61

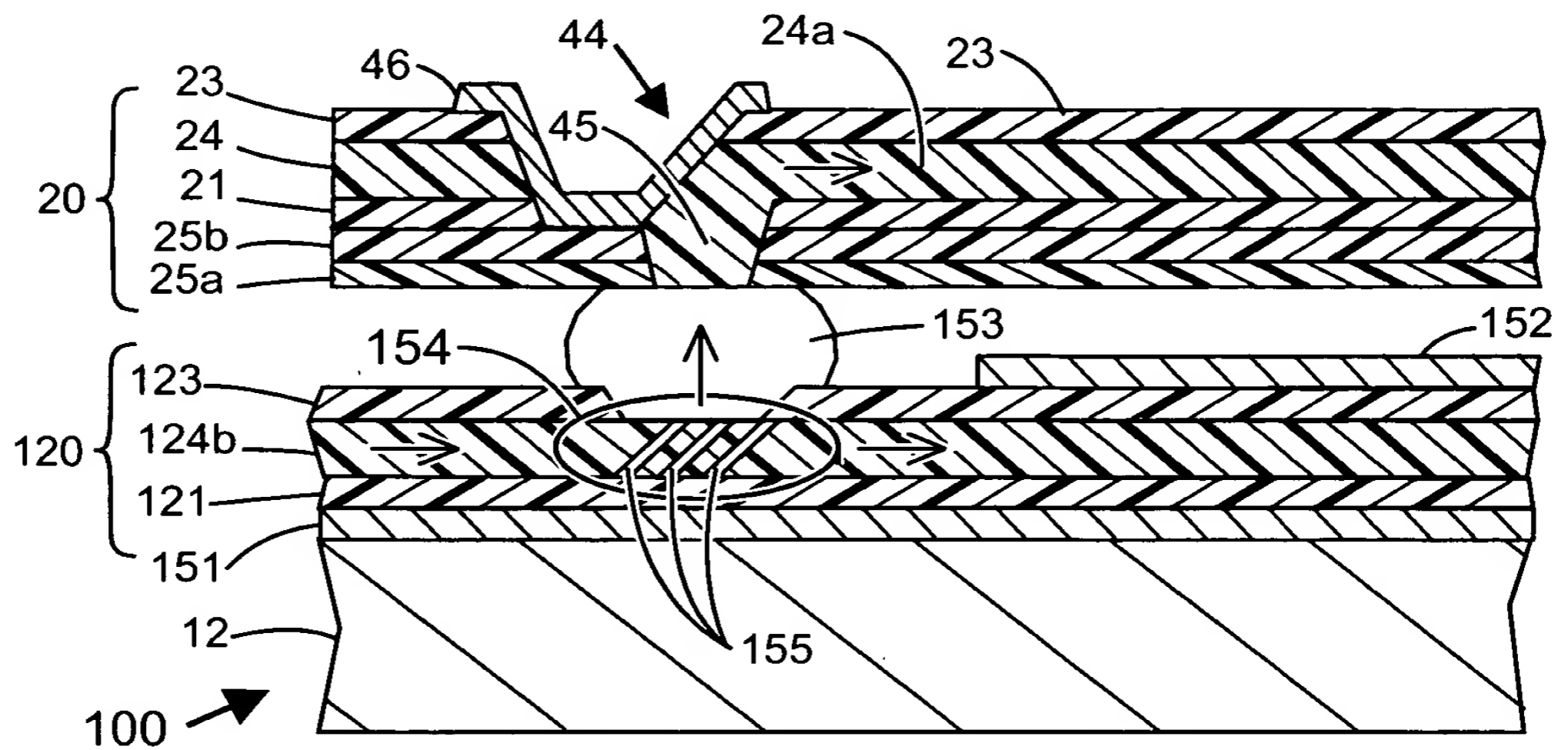
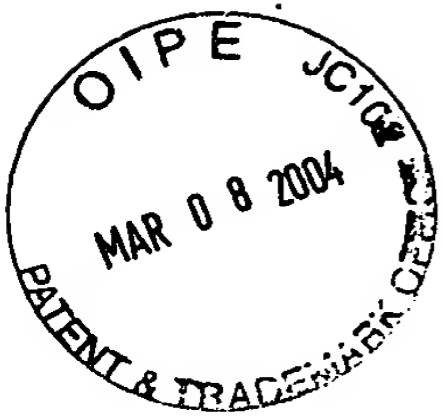


FIG. 22

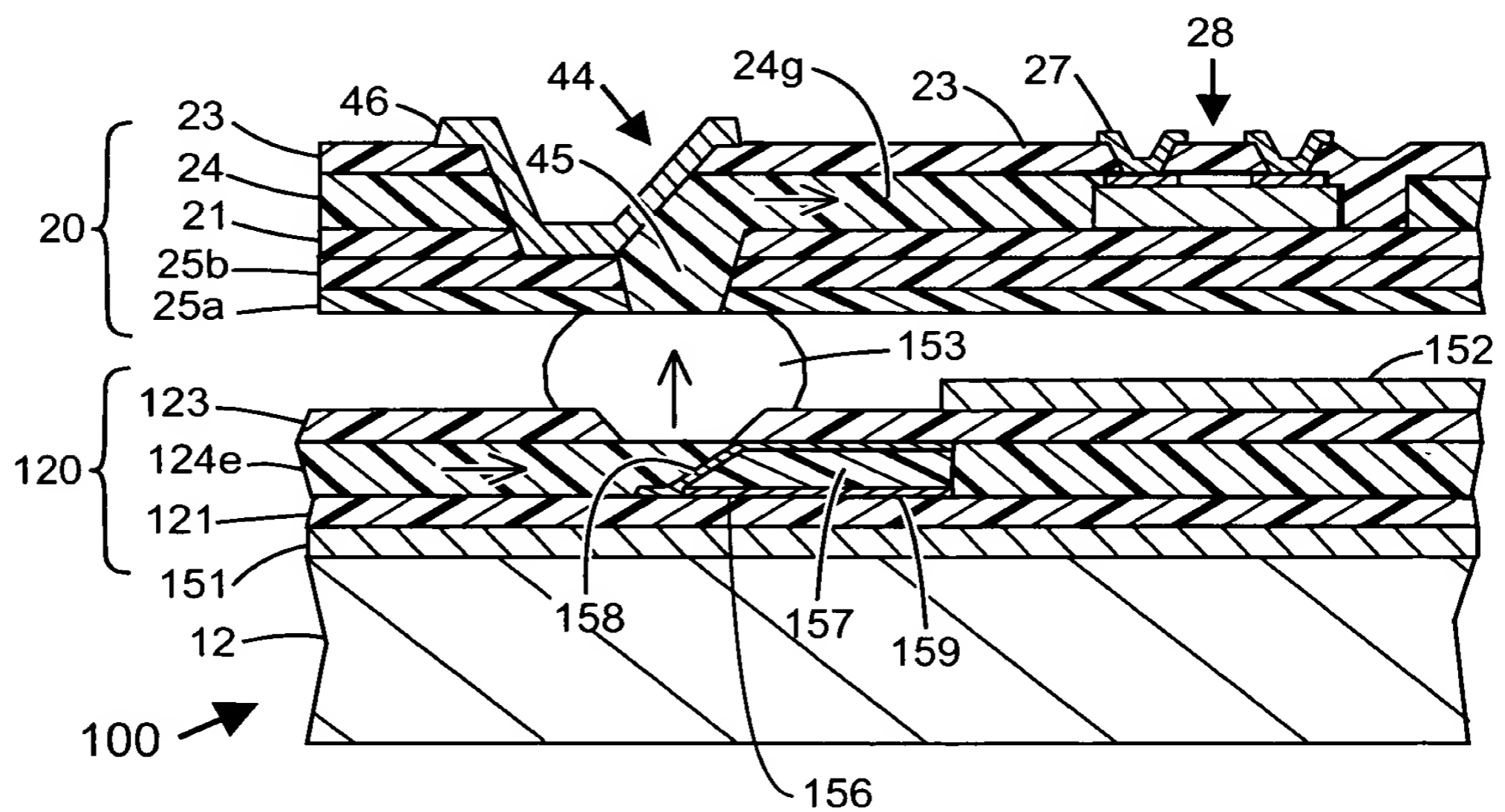


FIG. 23

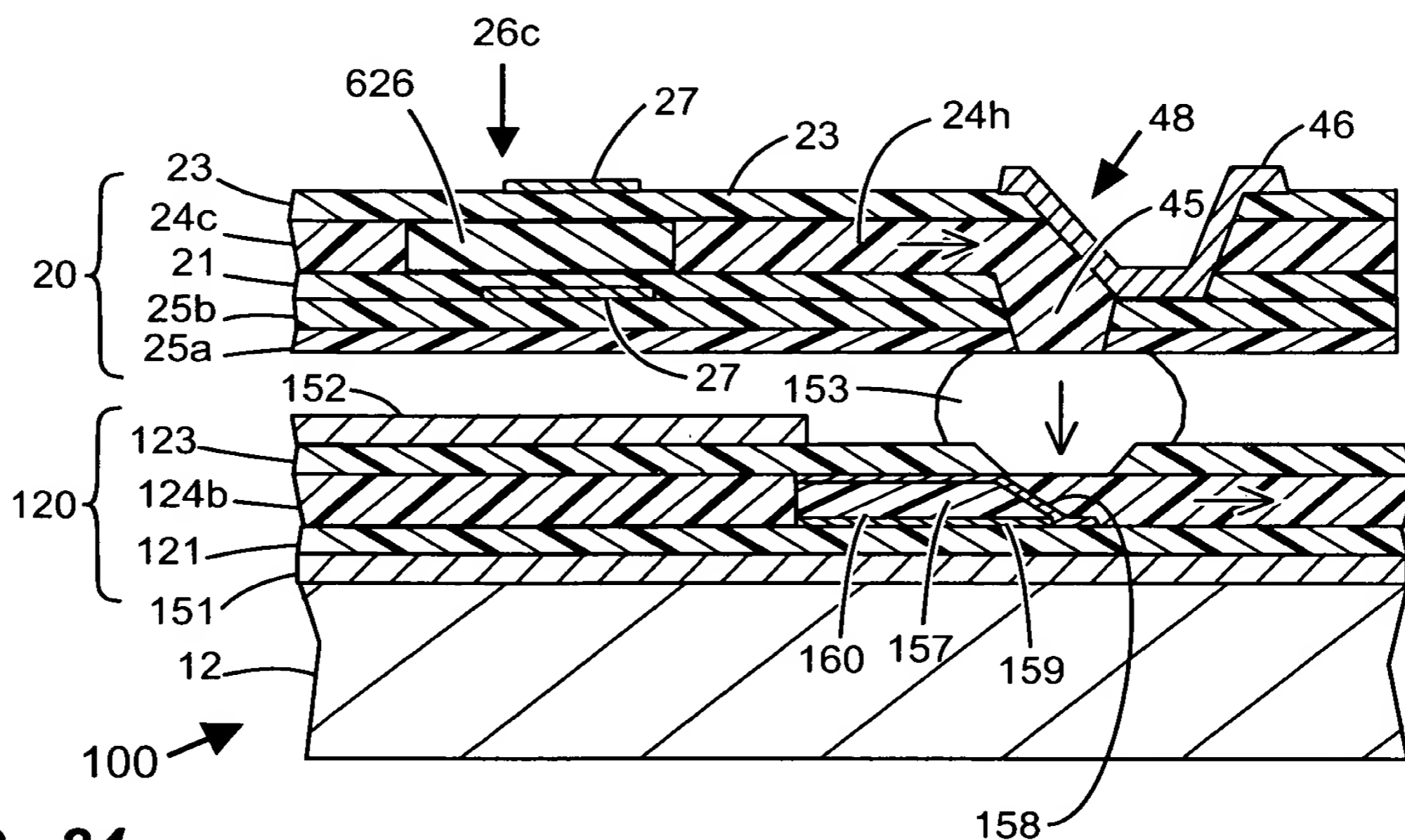


FIG. 24

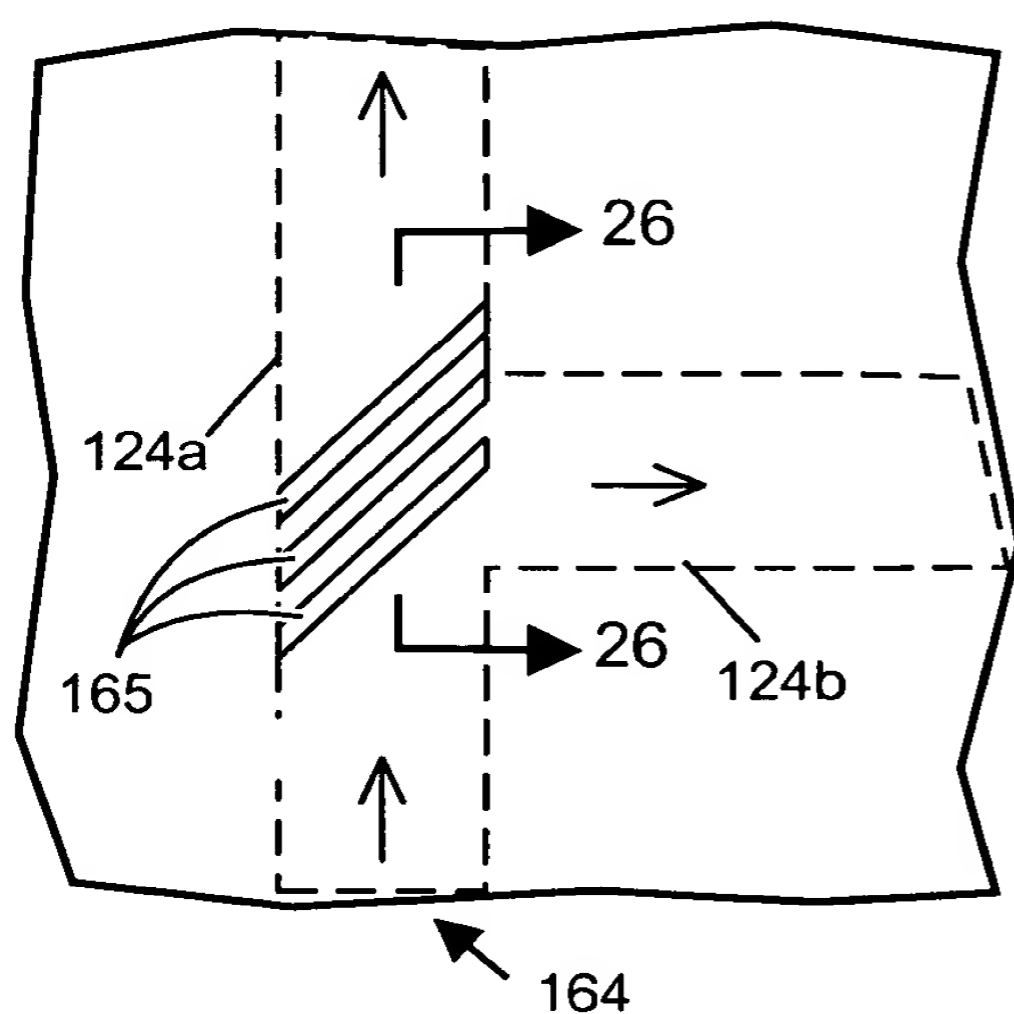


FIG. 25

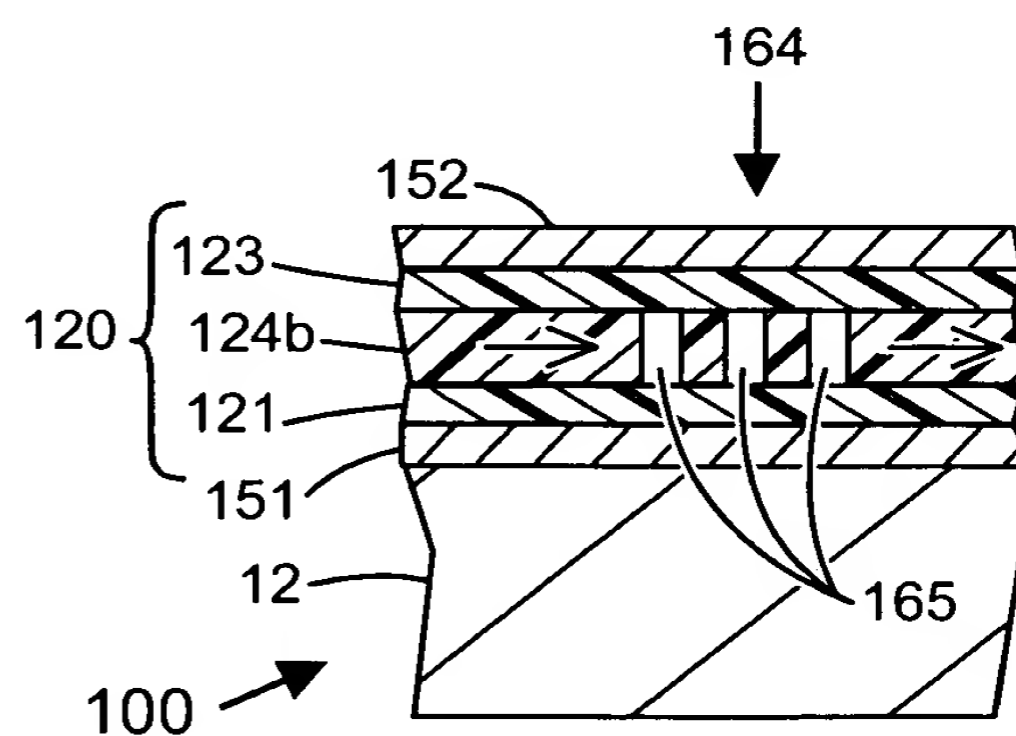
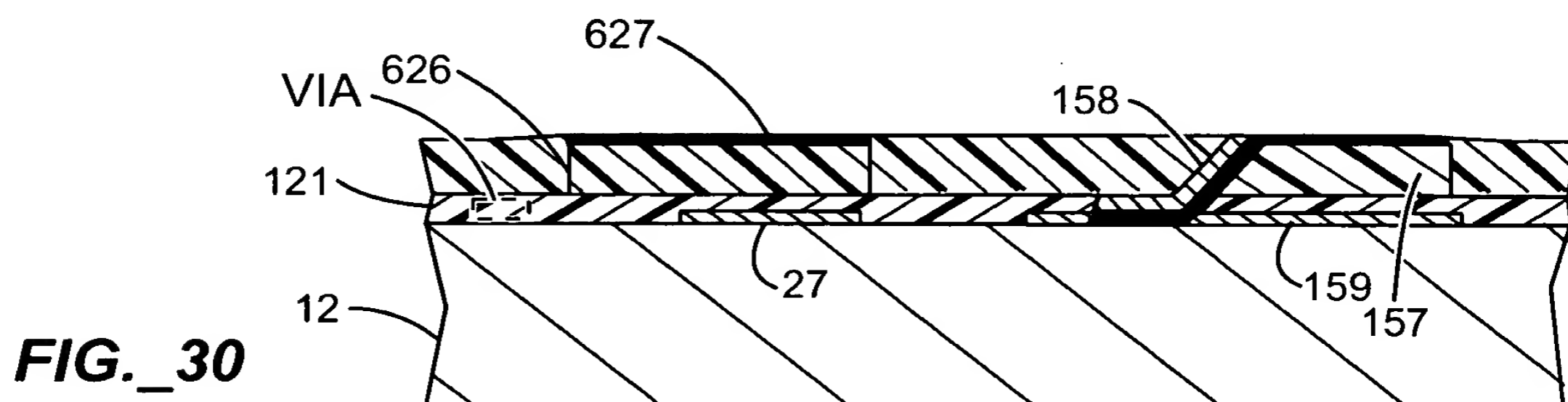
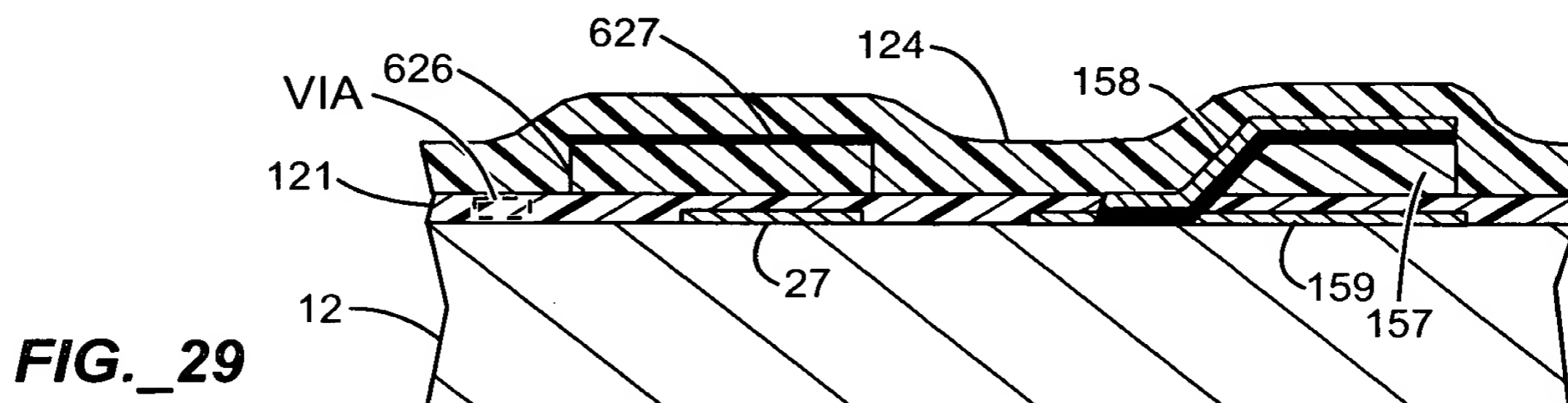
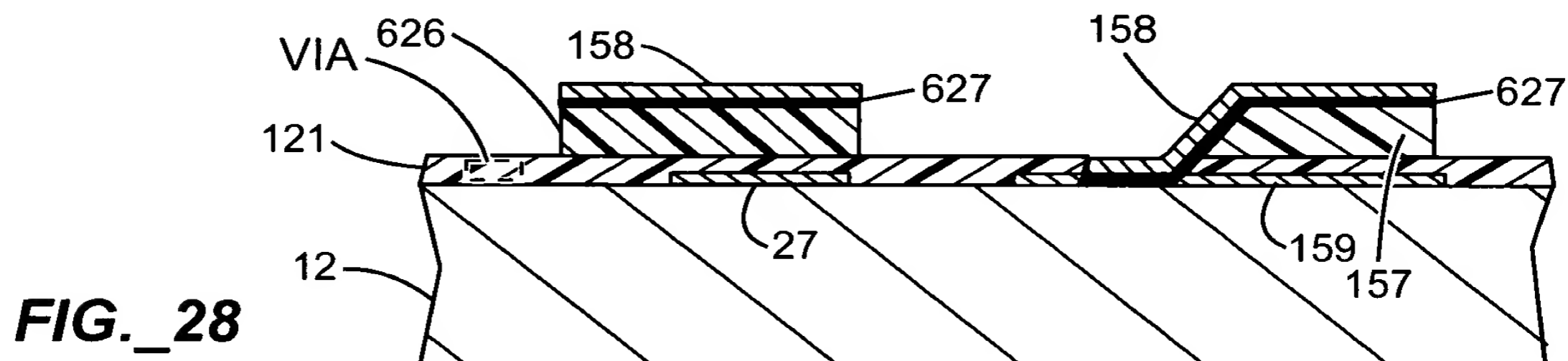
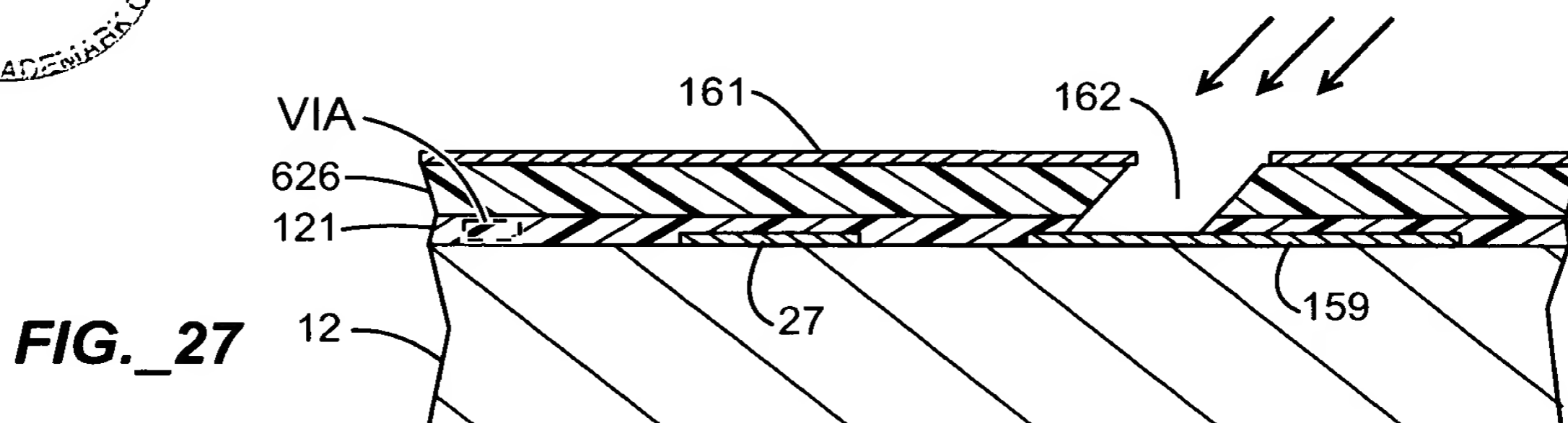


FIG. 26



14 / 61



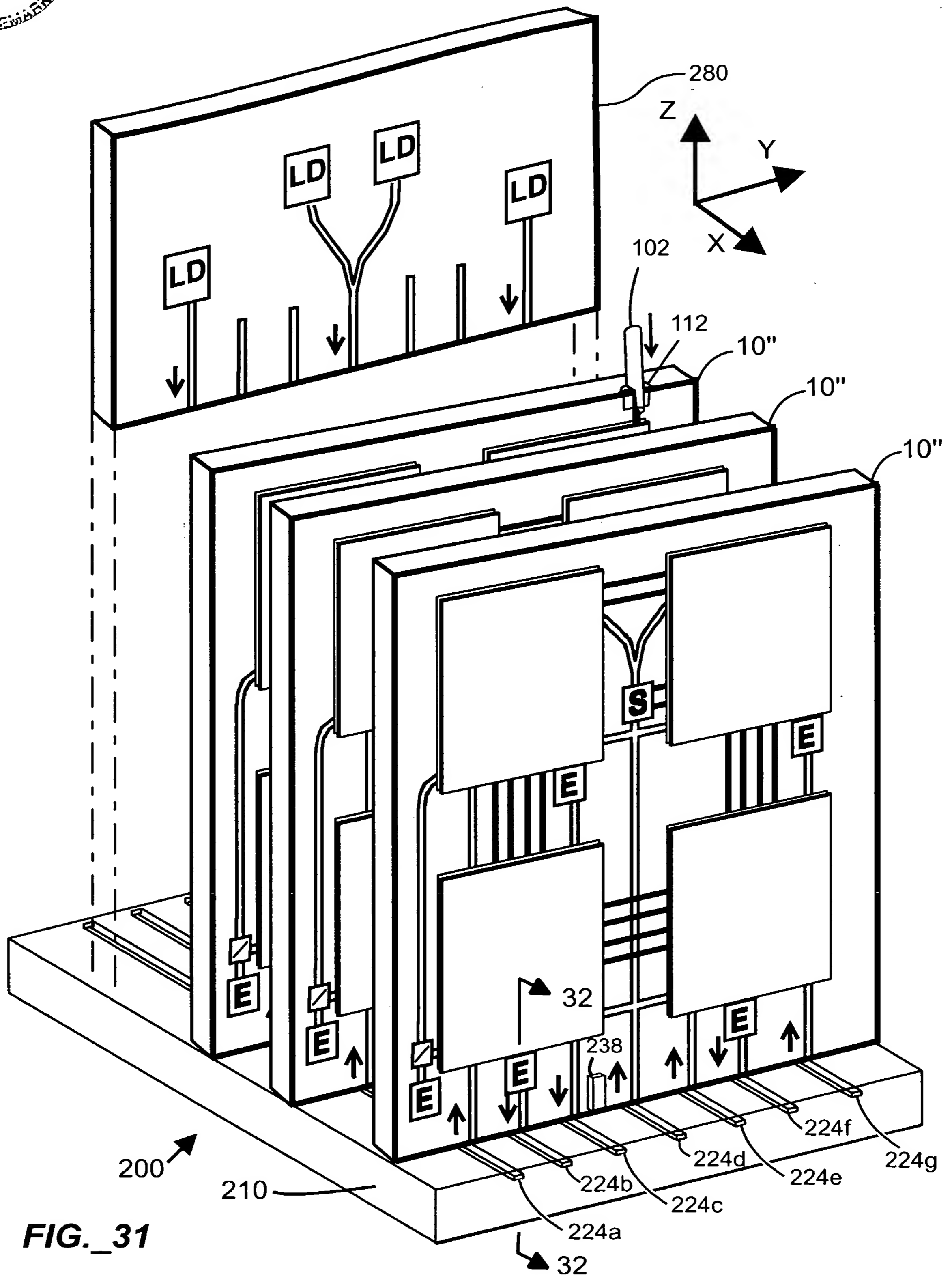


FIG. 31



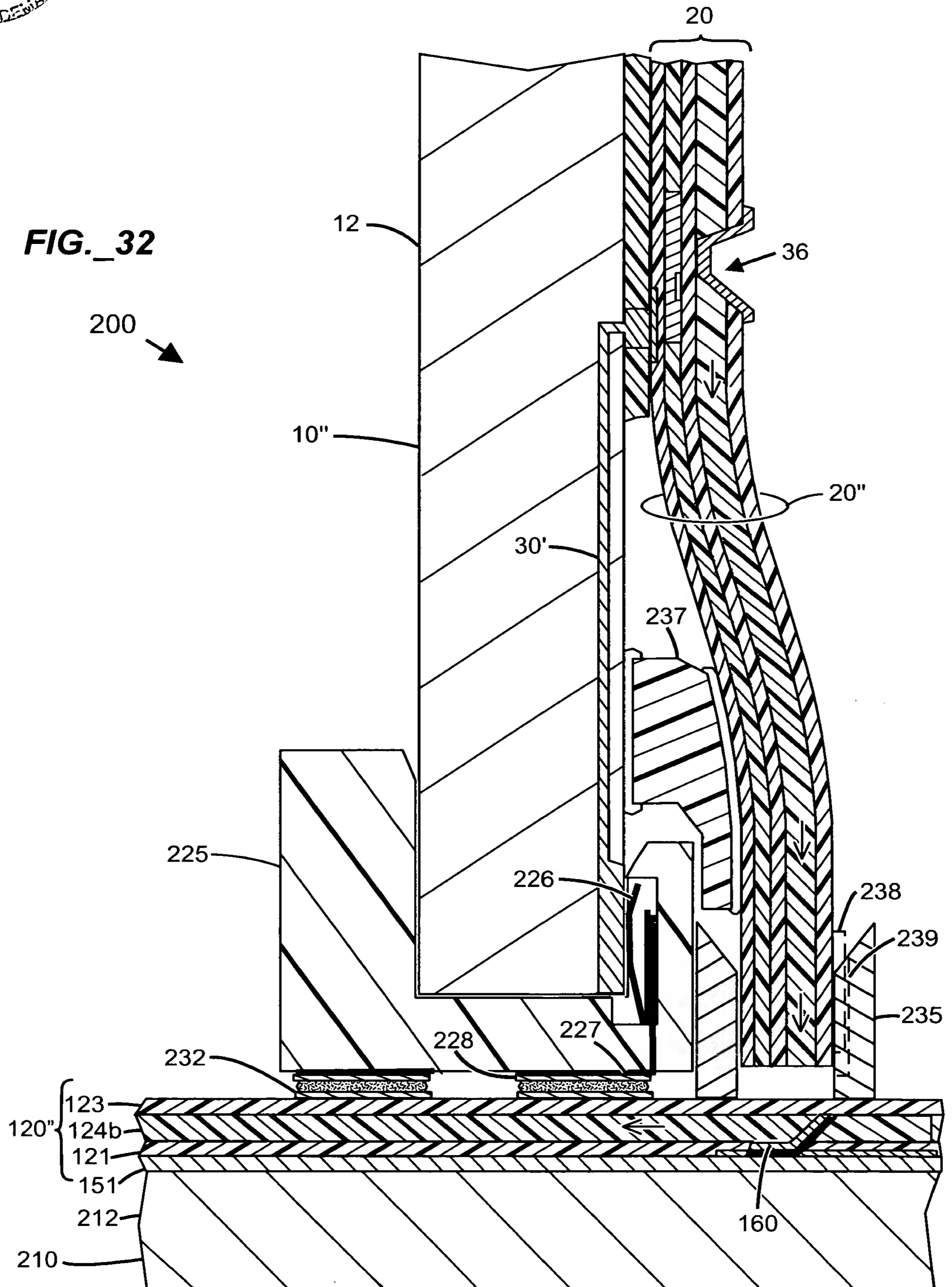
"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

16 / 61

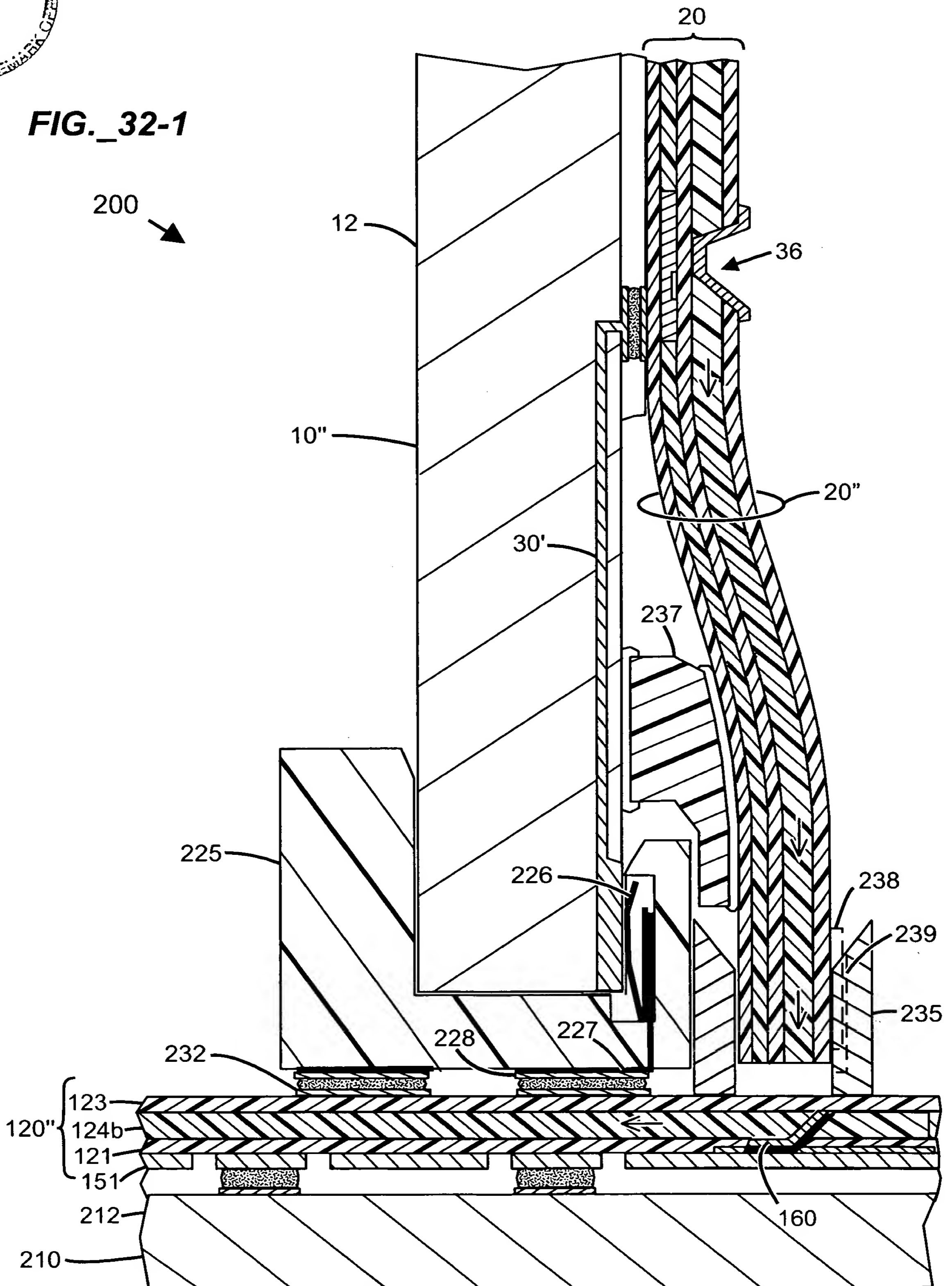
FIG. 32

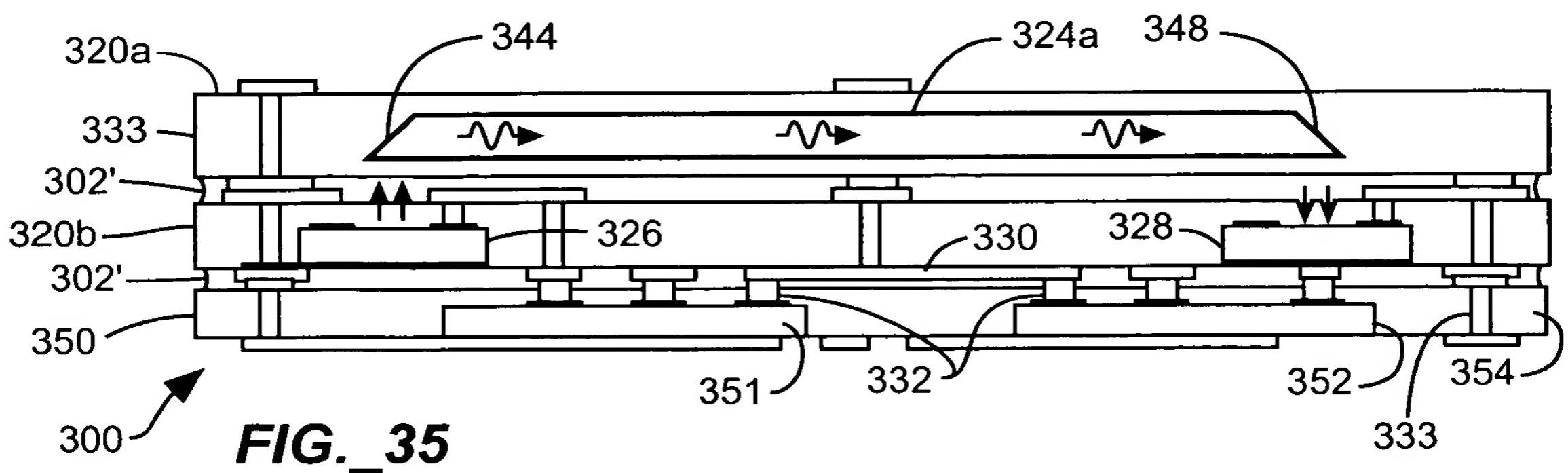
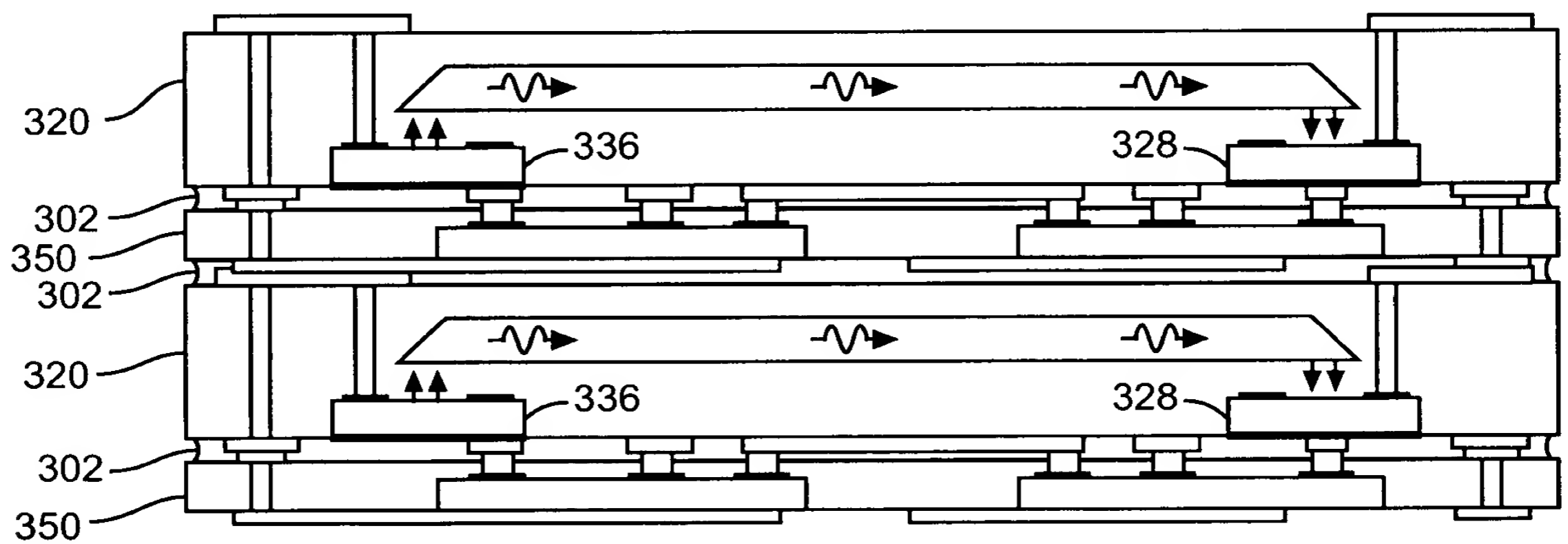
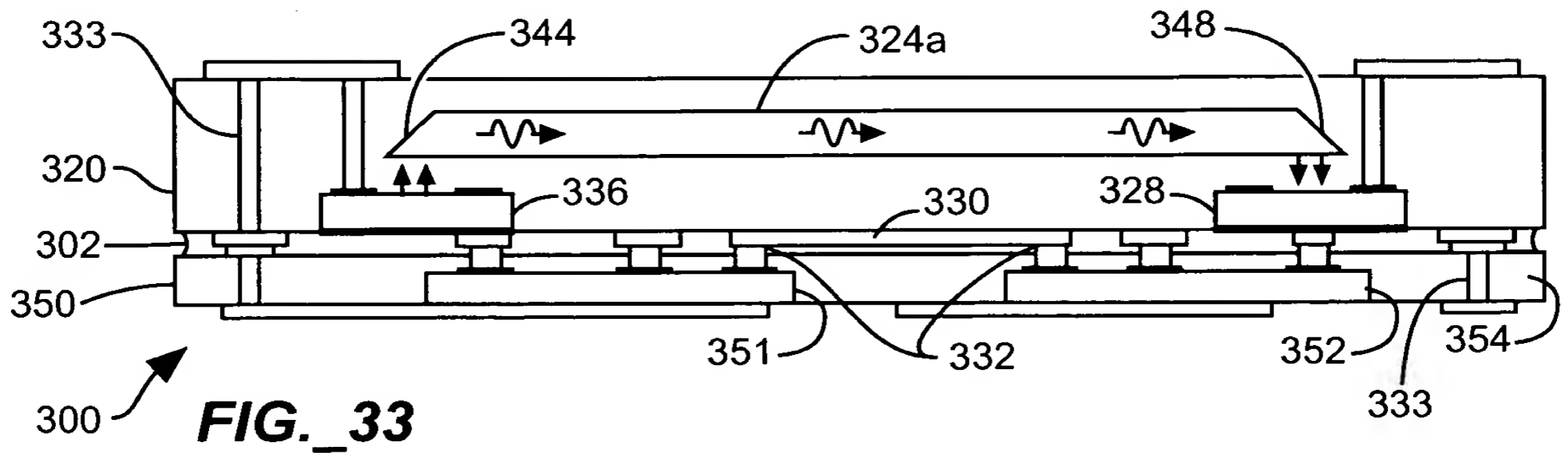
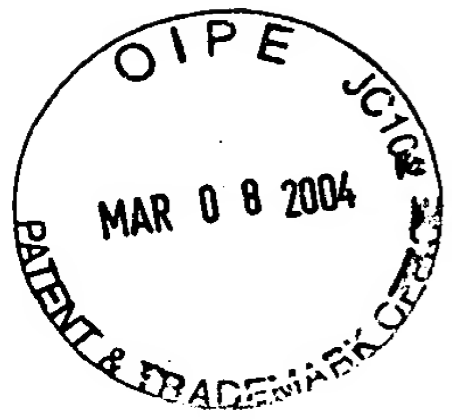




17 / 61

FIG._32-1





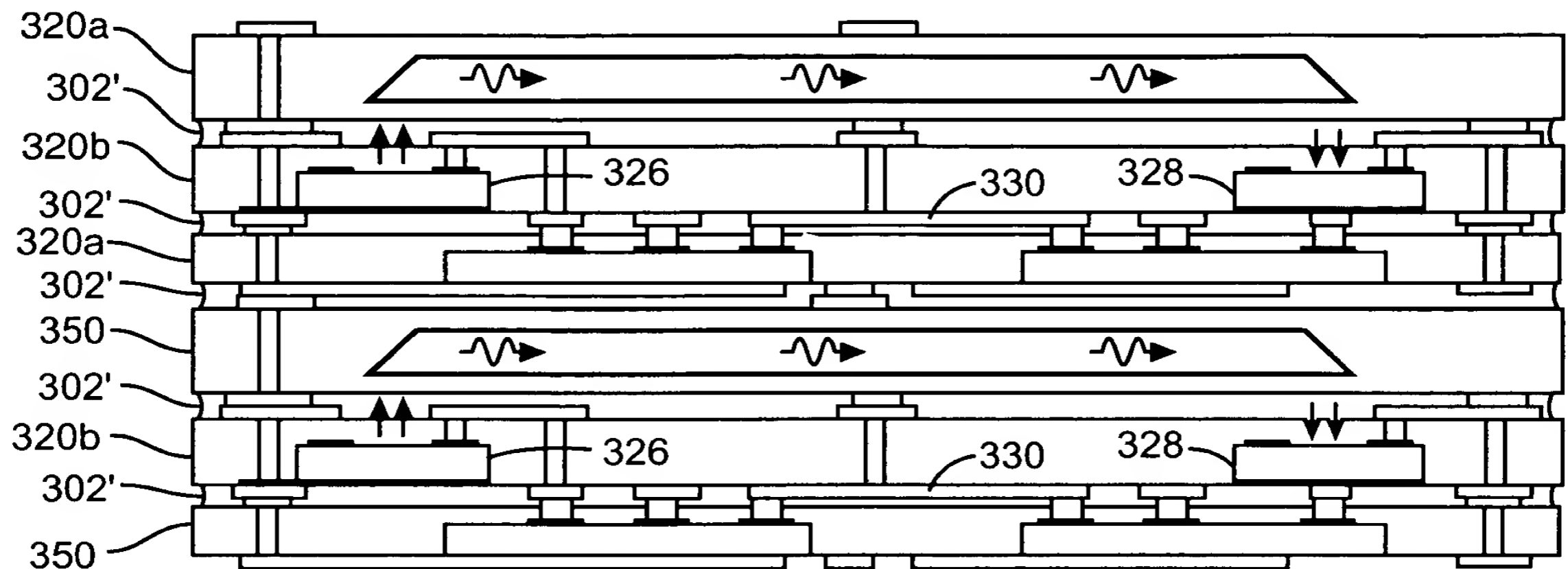


FIG. 36

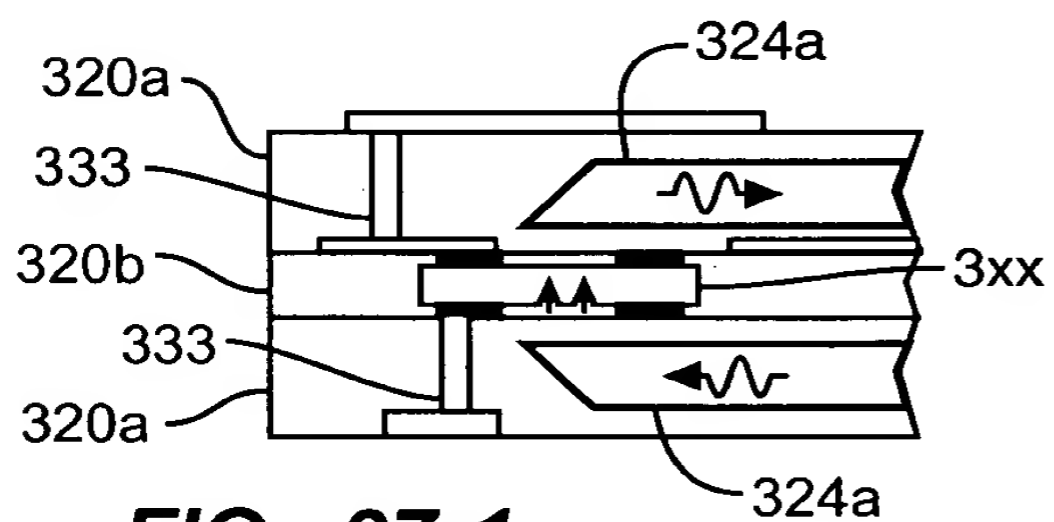


FIG. 37-1

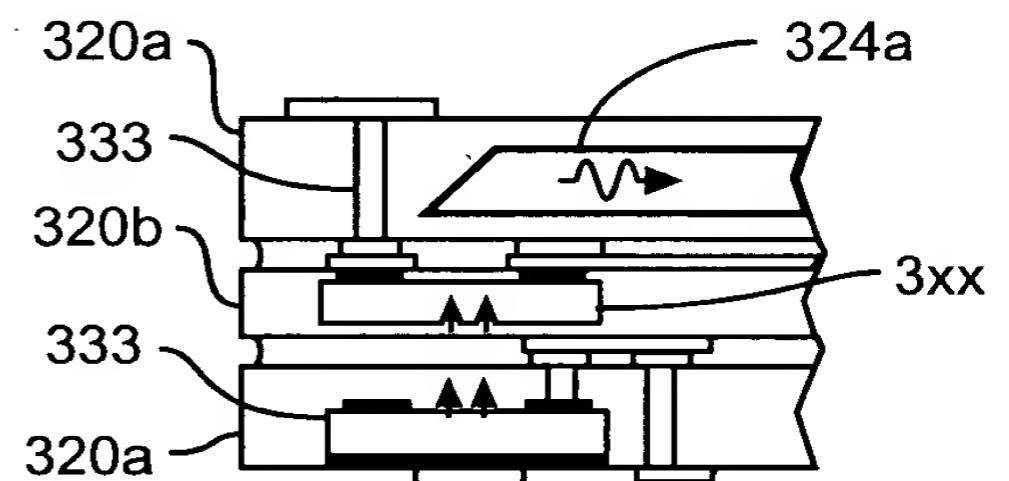


FIG. 37-2

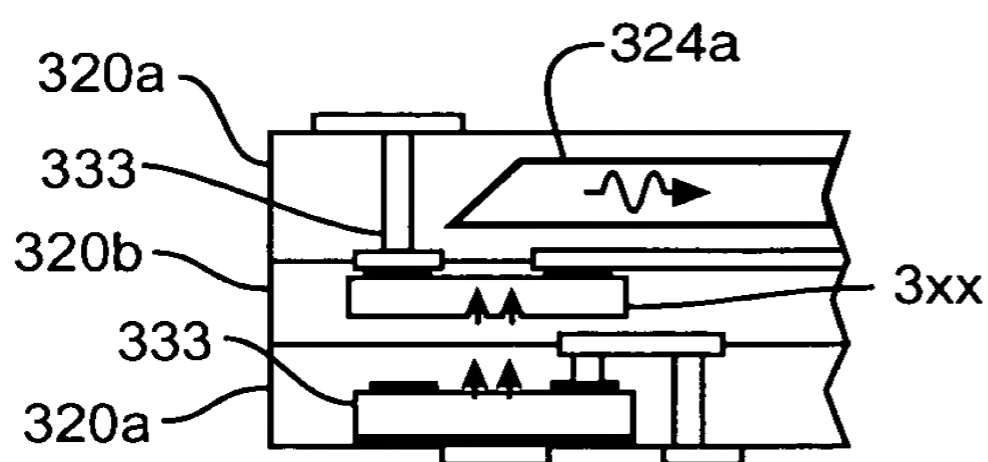


FIG. 37-3

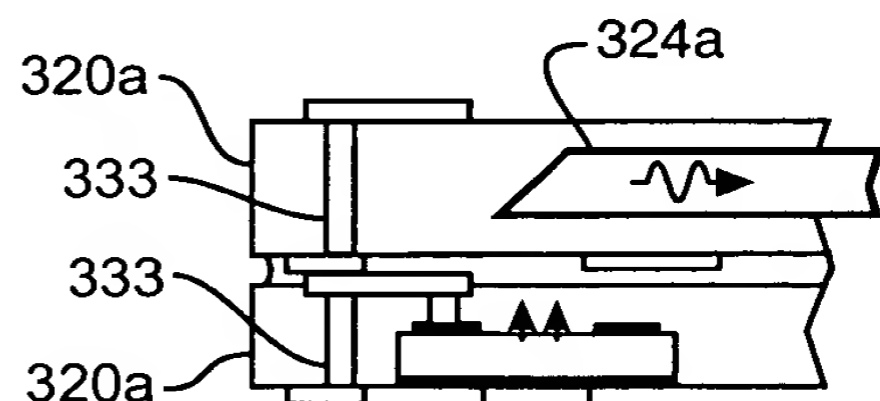


FIG. 37-4



"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

20 / 61

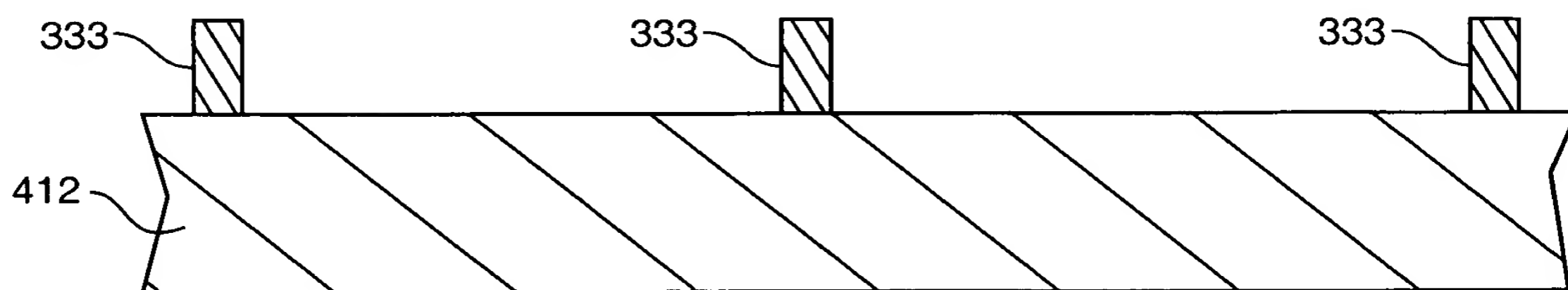


FIG._38

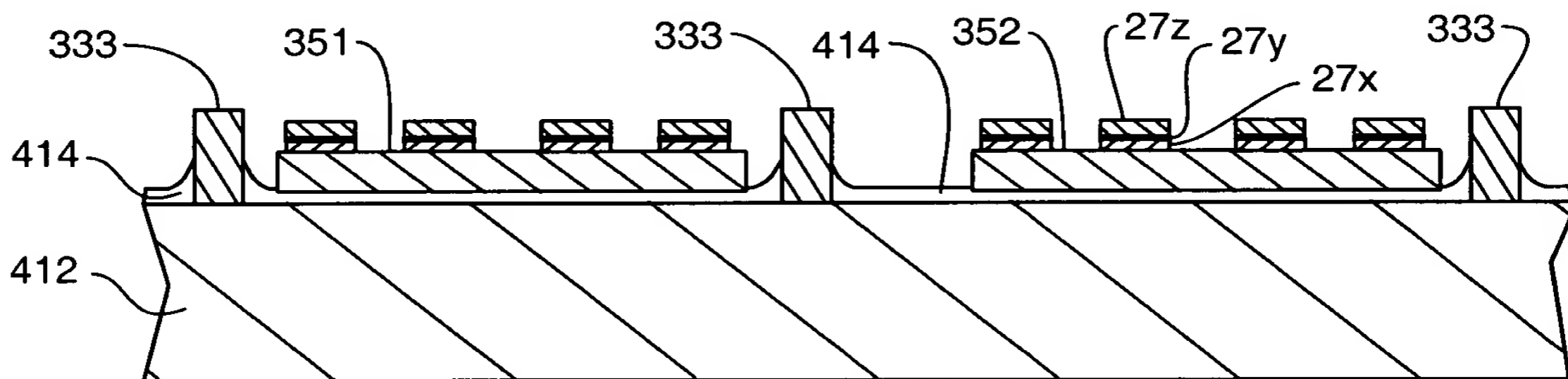


FIG._39

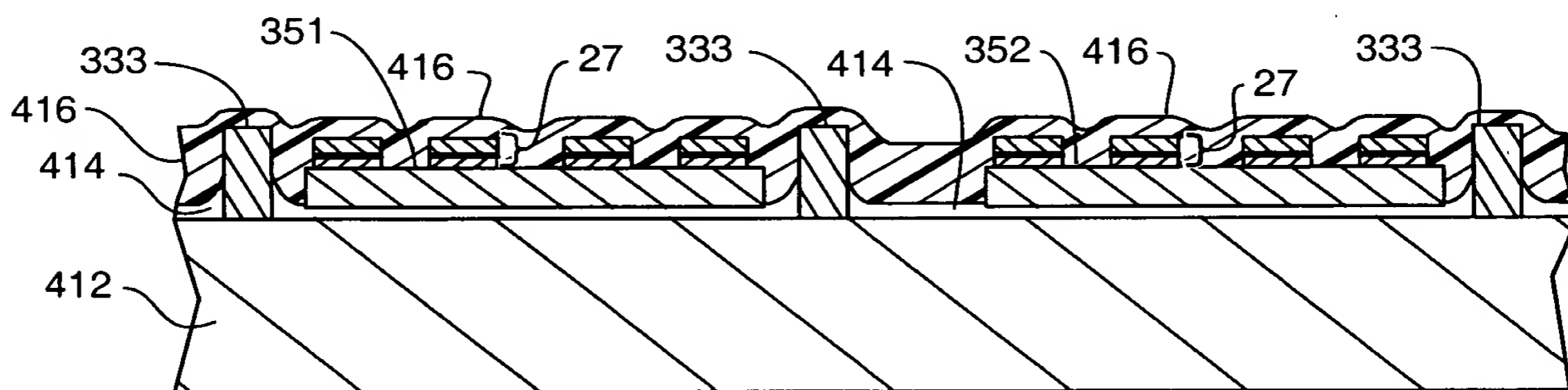


FIG._40

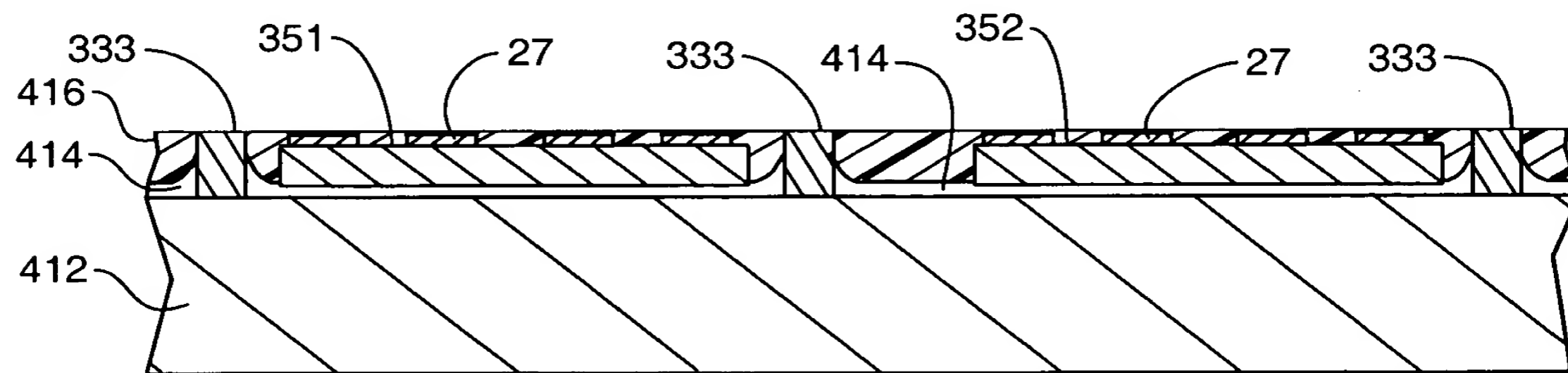


FIG._41

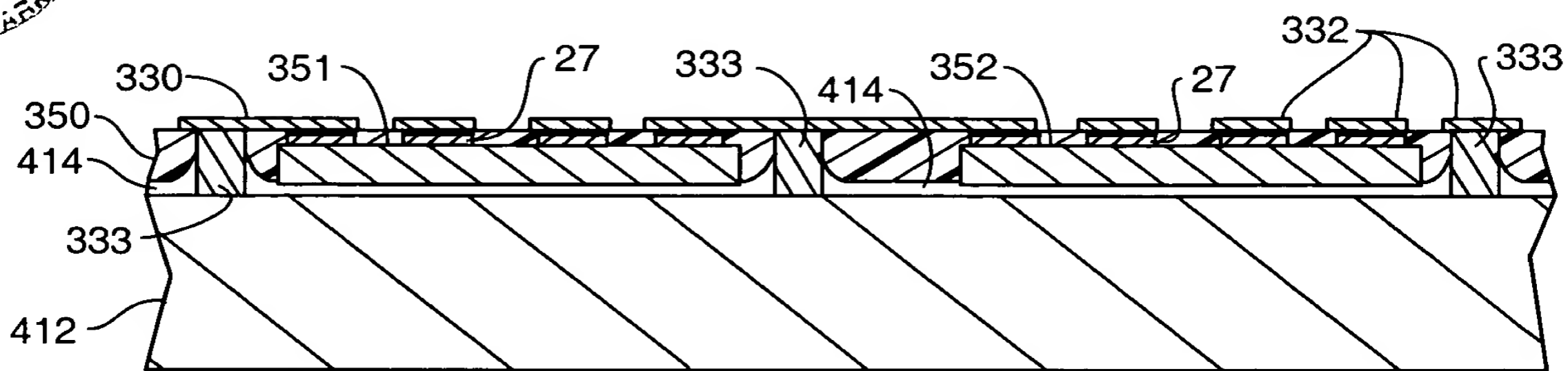


FIG. 42

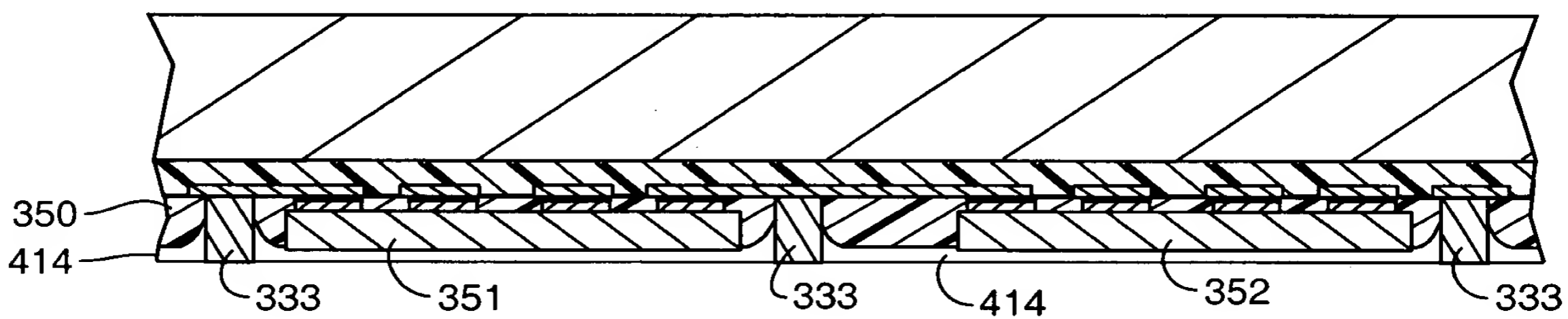


FIG. 43

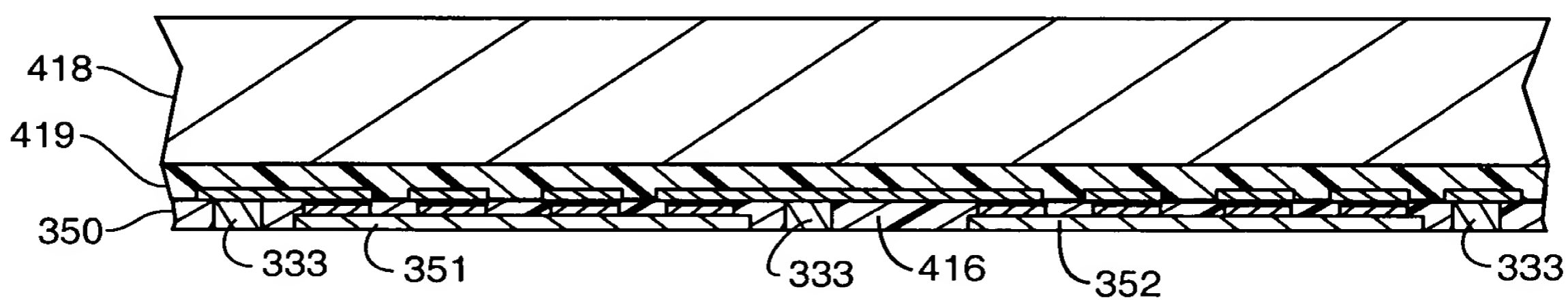


FIG. 44

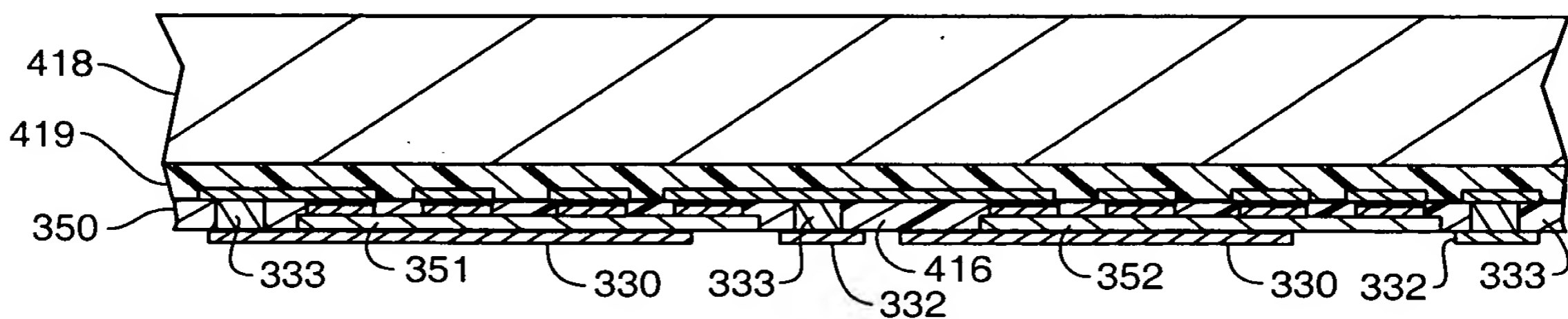
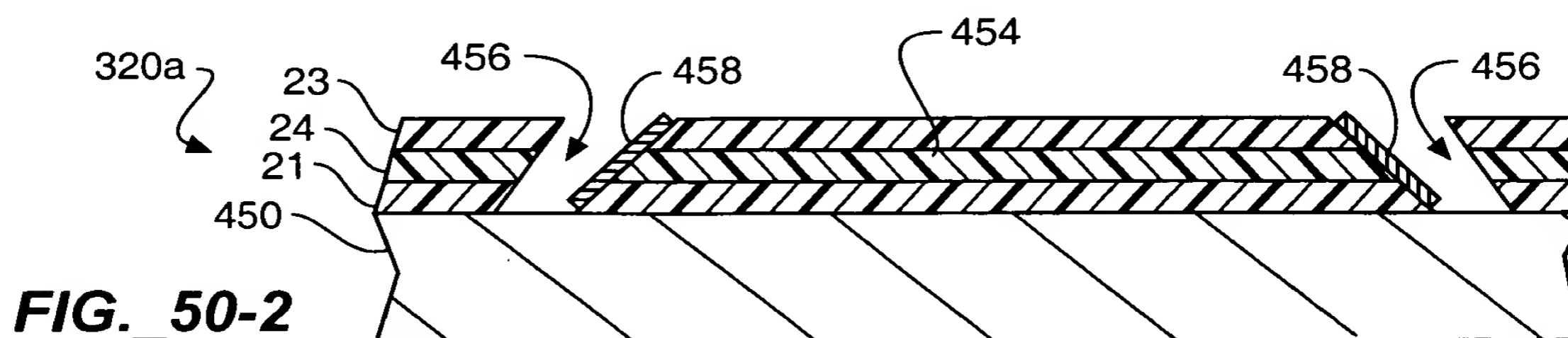
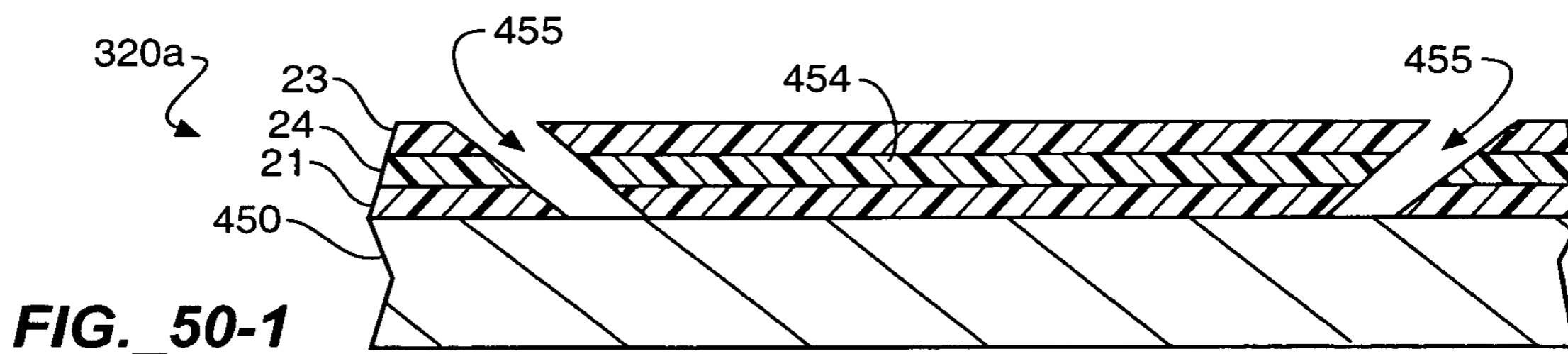
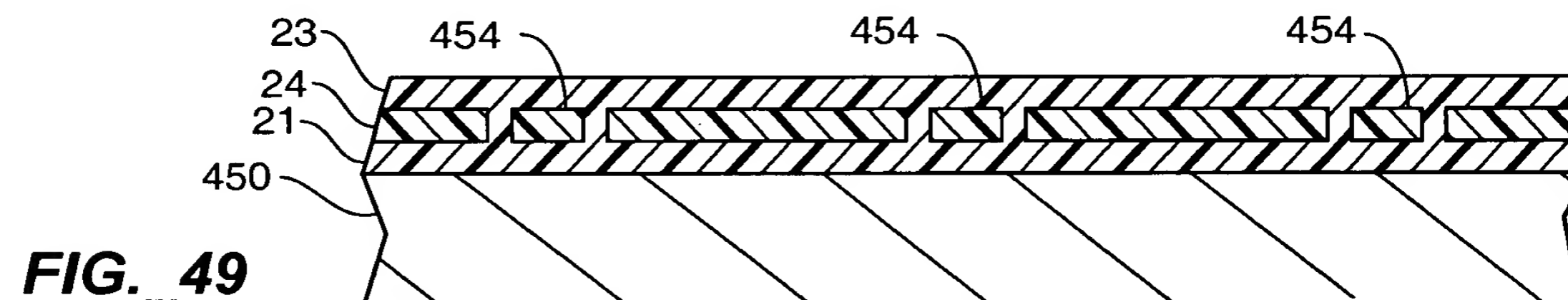
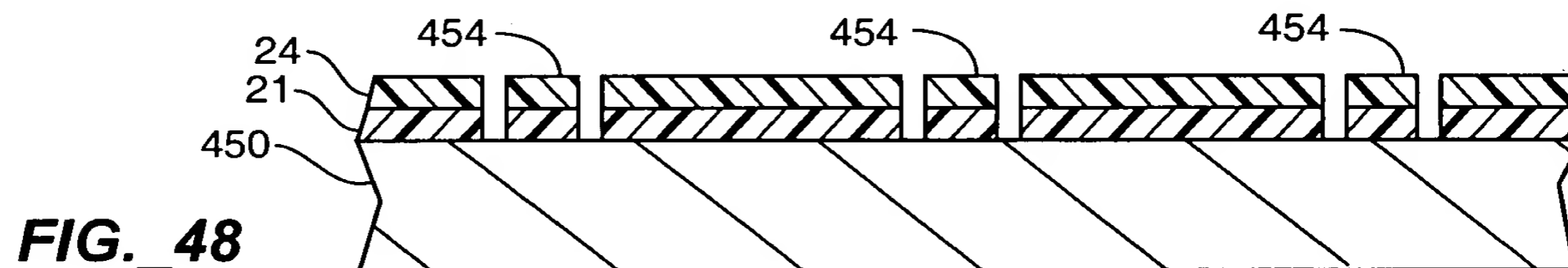
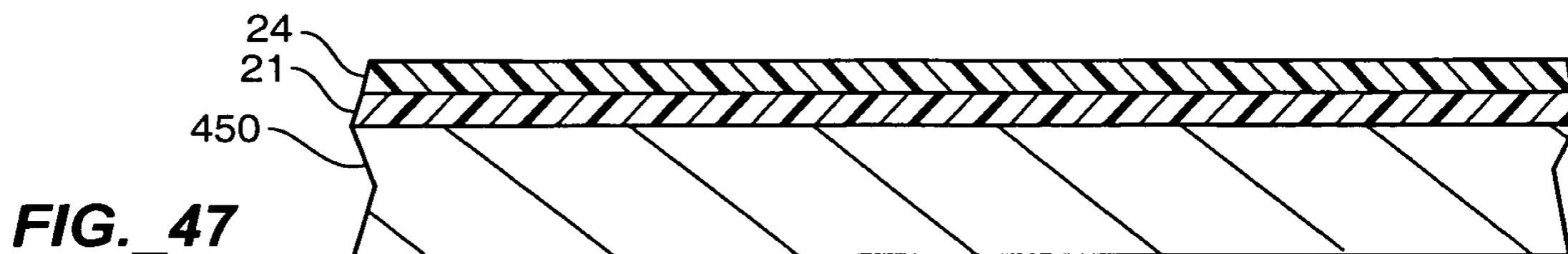
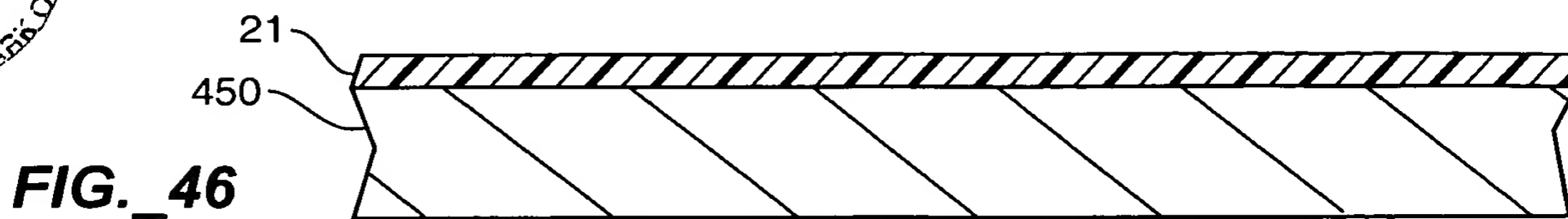
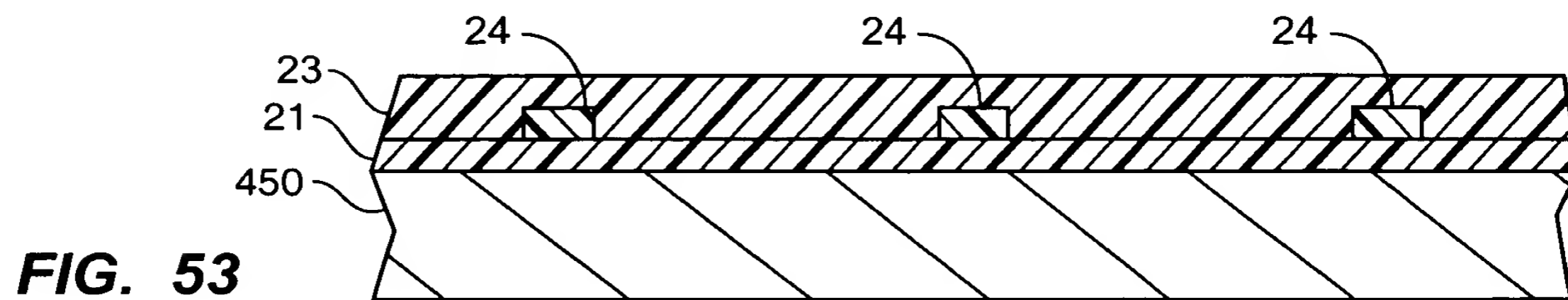
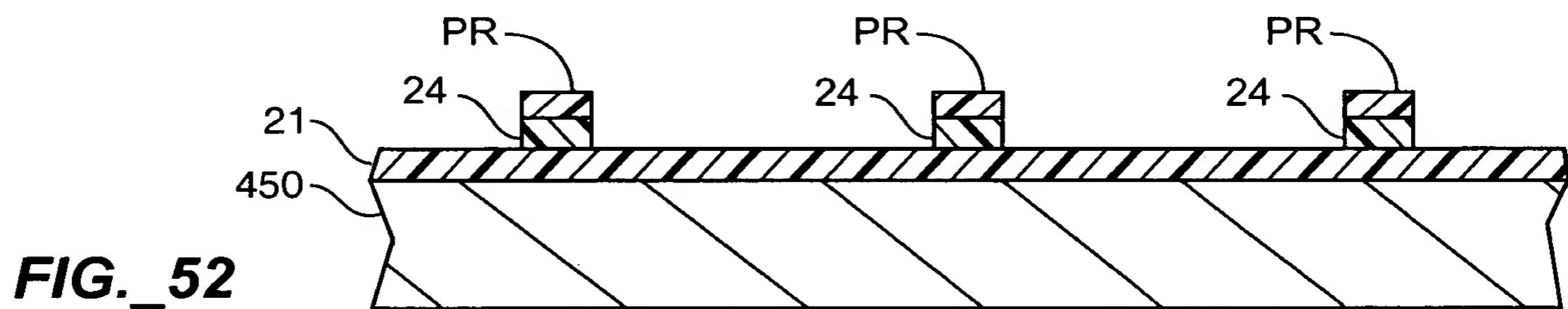
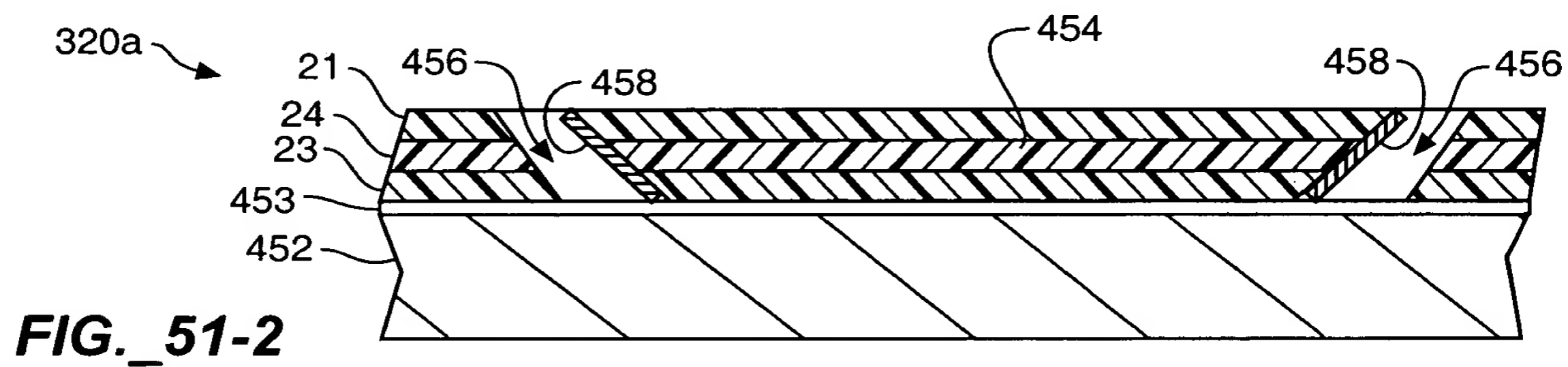
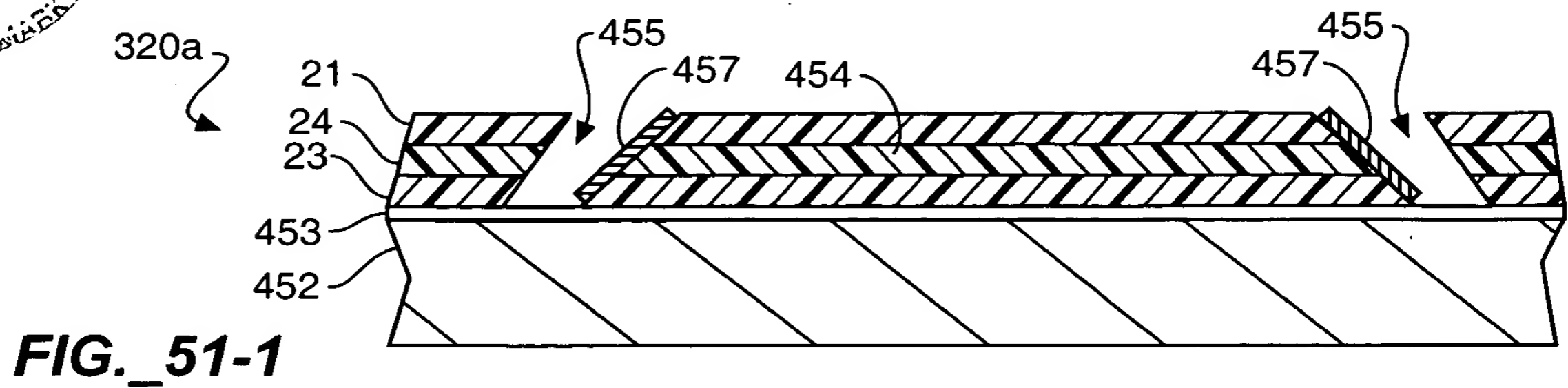
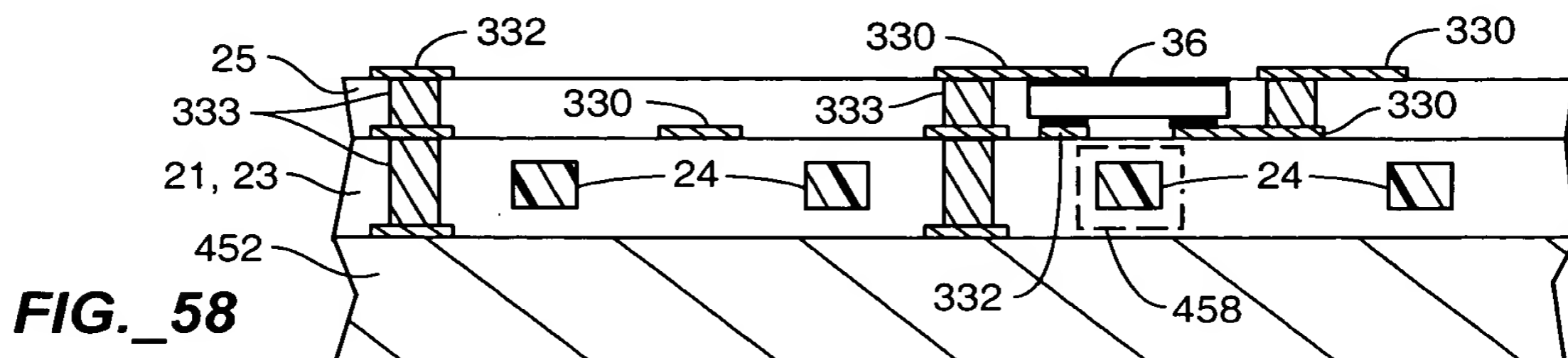
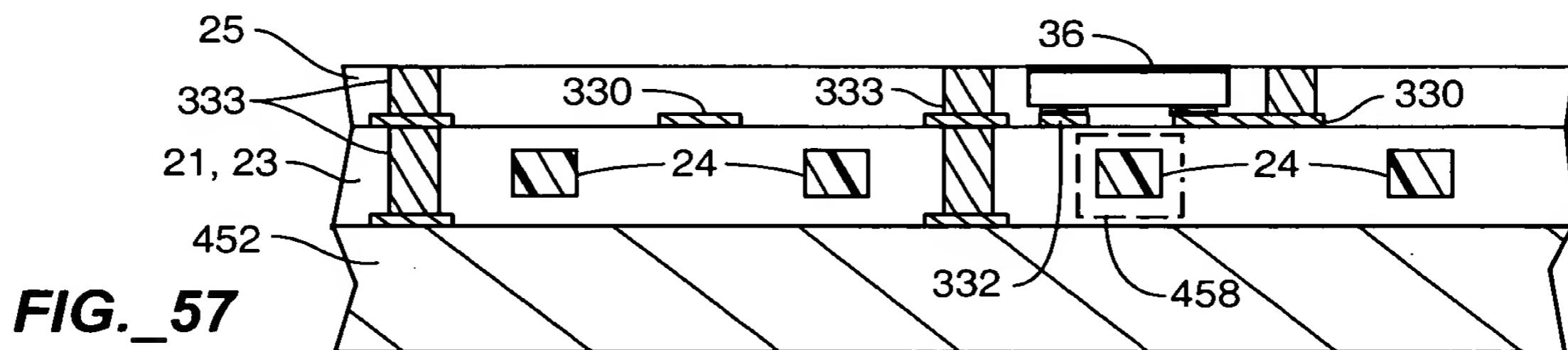
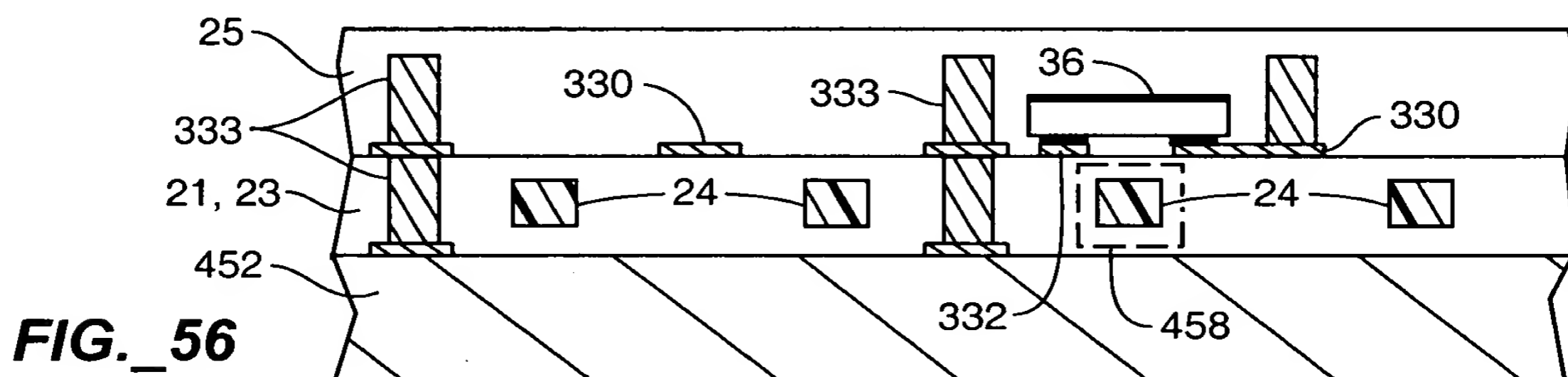
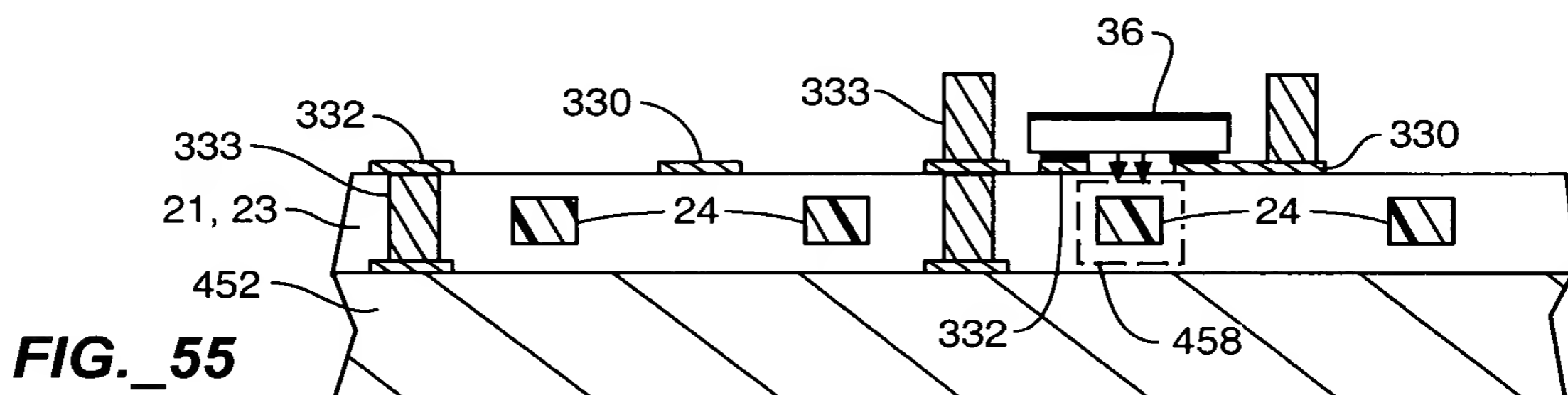
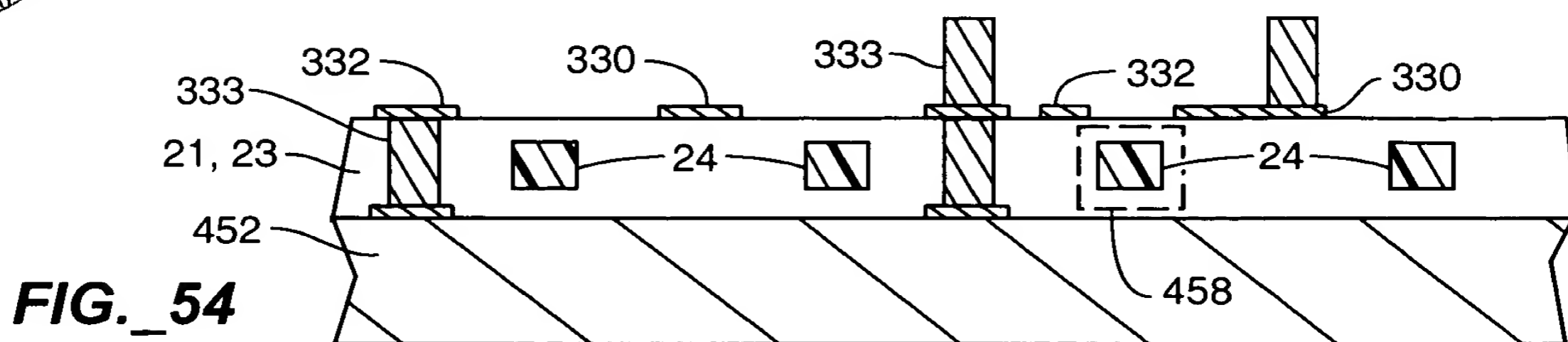


FIG. 45







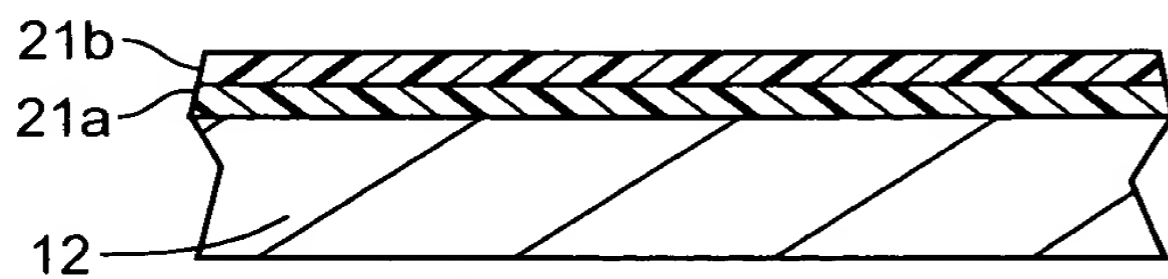


FIG. 59

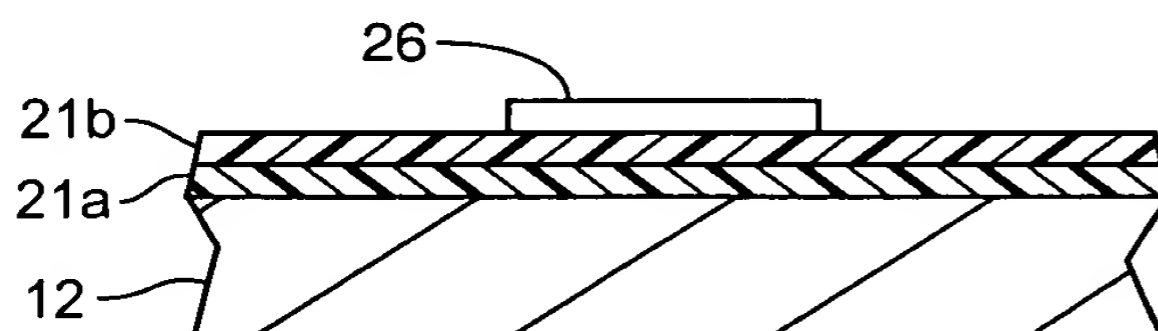


FIG. 60

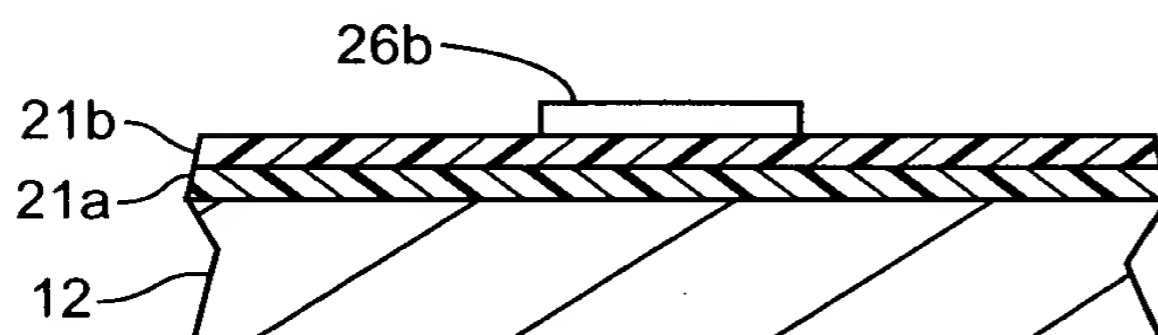


FIG. 62

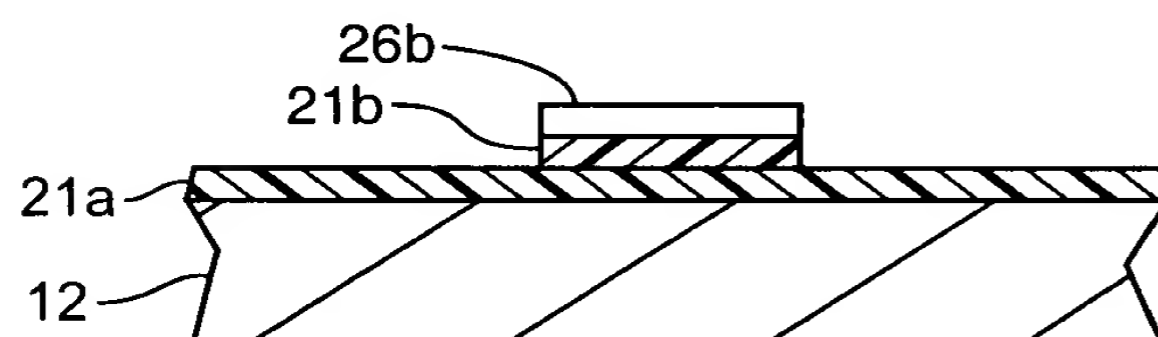


FIG. 64

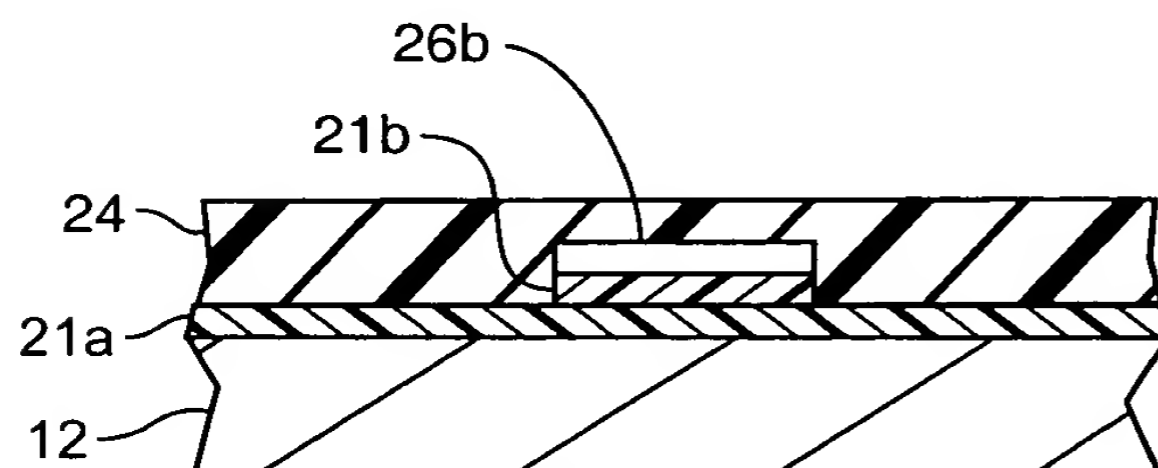


FIG. 65

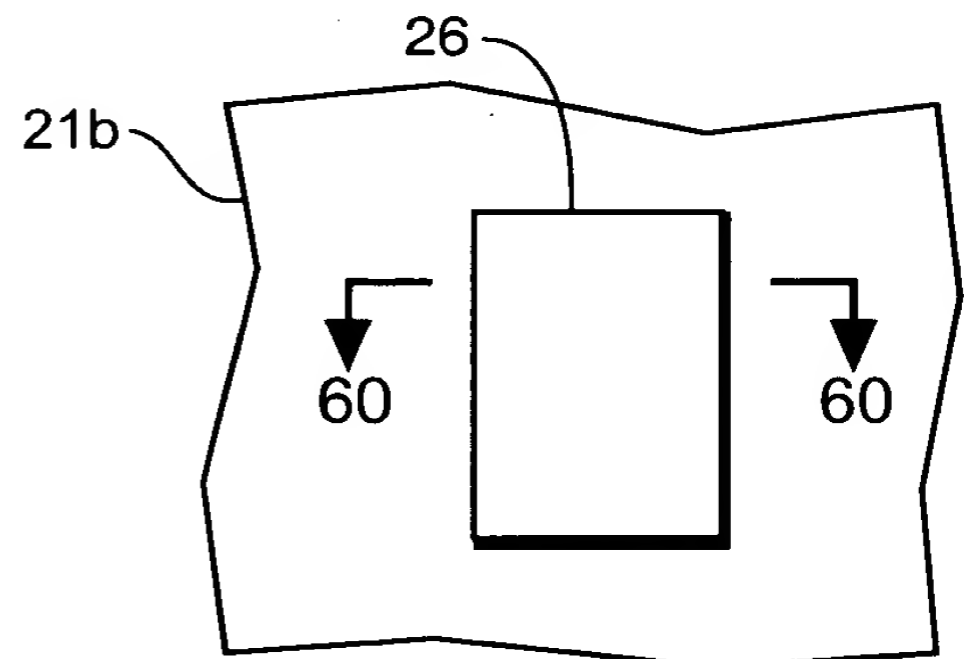


FIG. 61

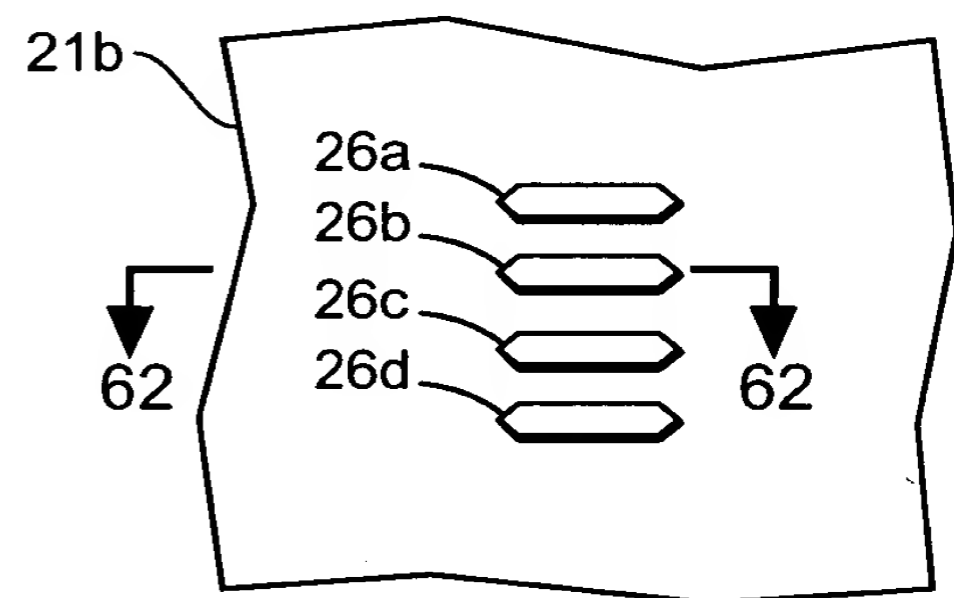
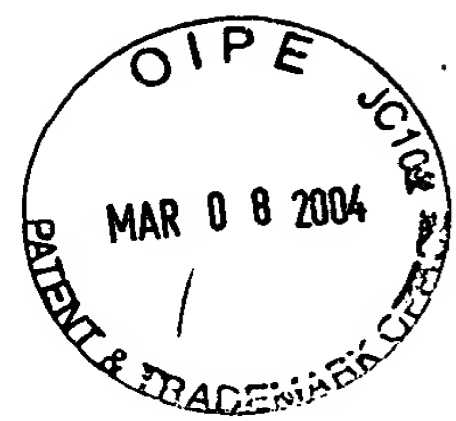


FIG. 63



26 / 61

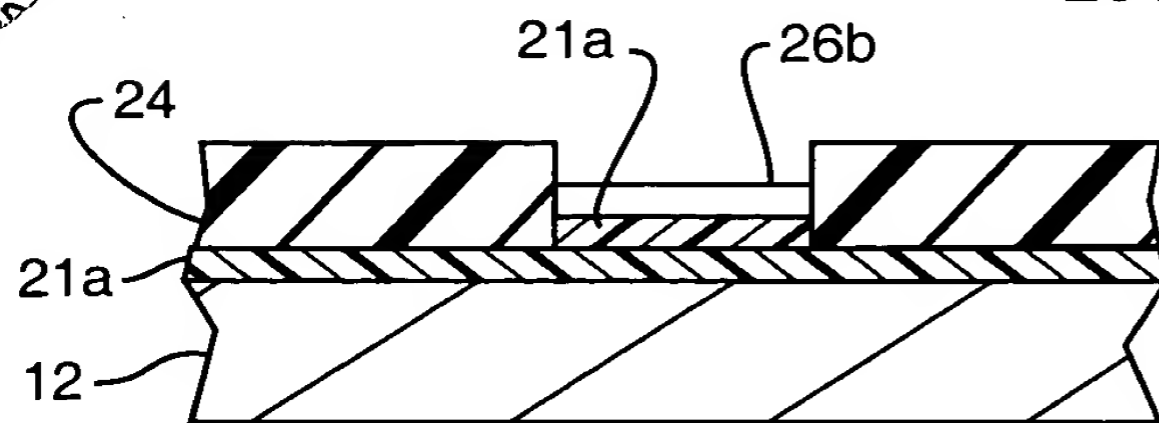


FIG._66

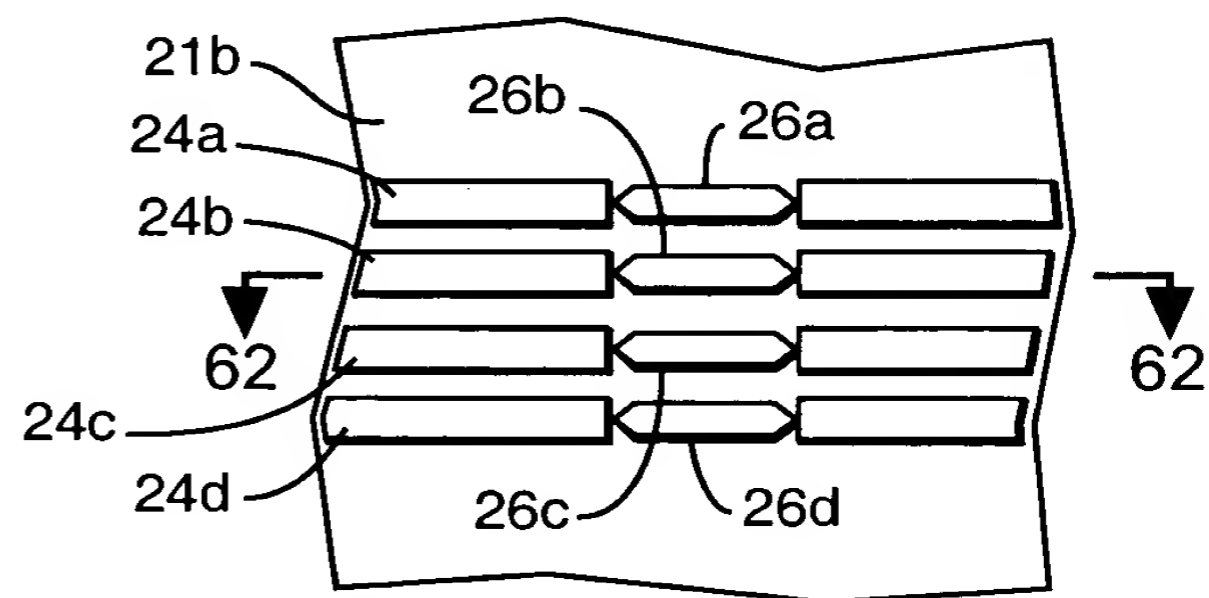


FIG._67

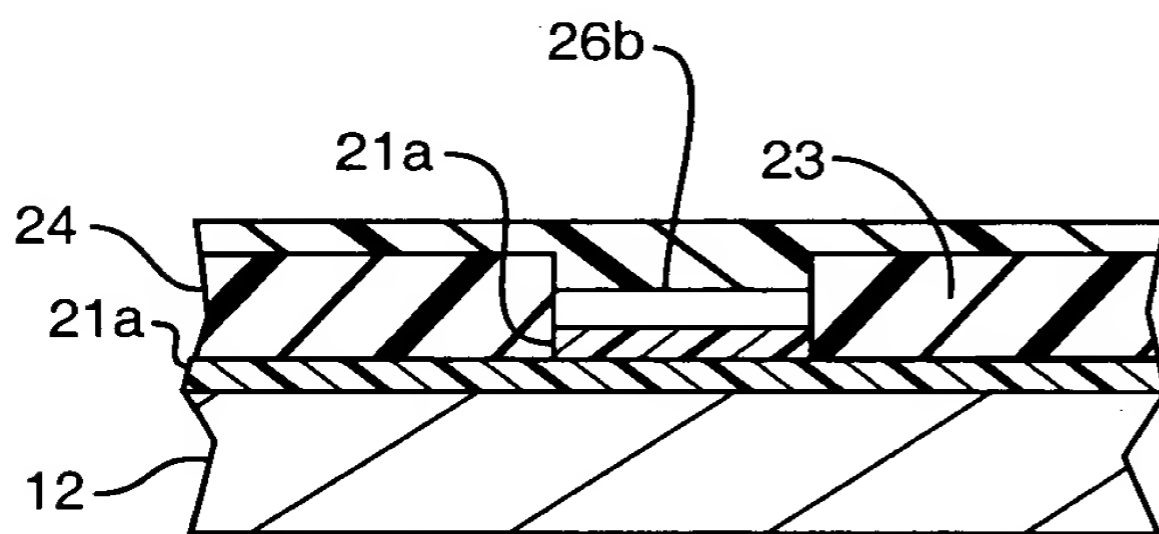


FIG._68

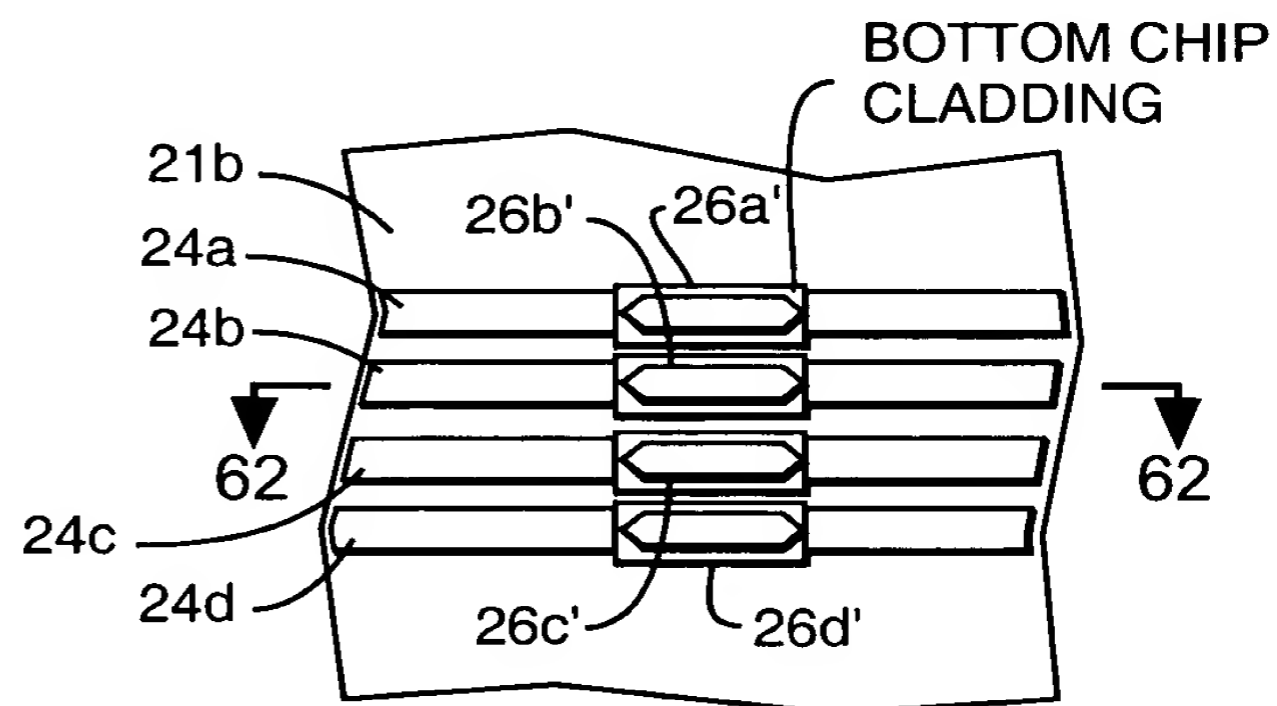


FIG._67-2

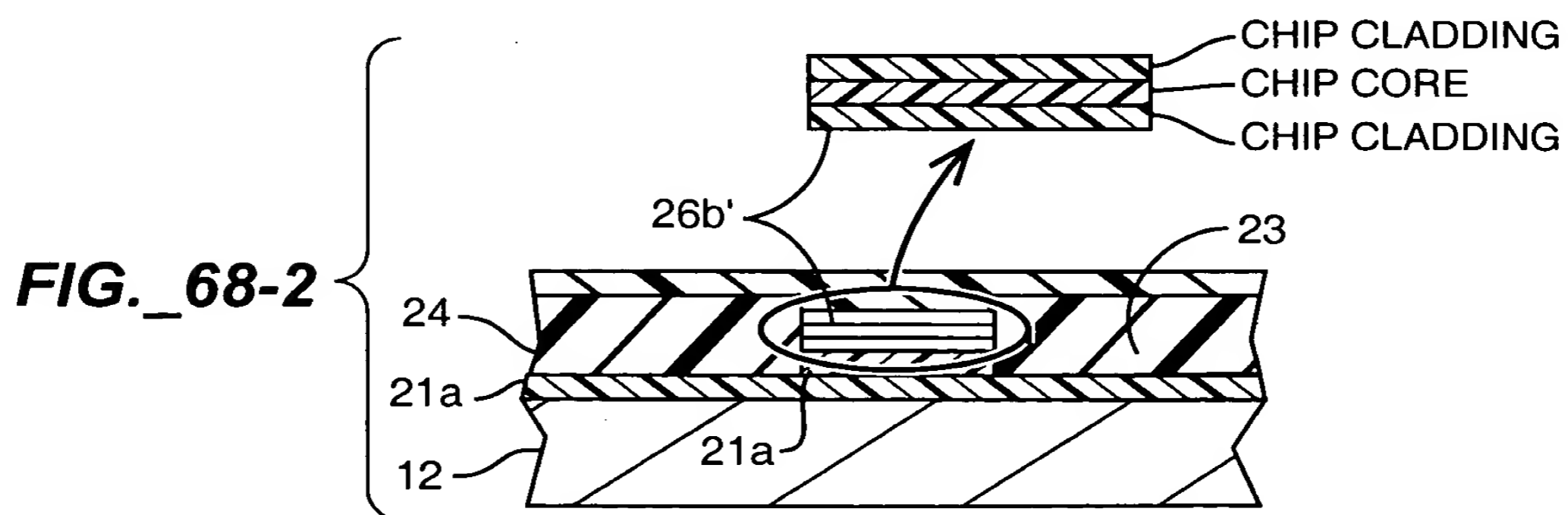


FIG._68-2

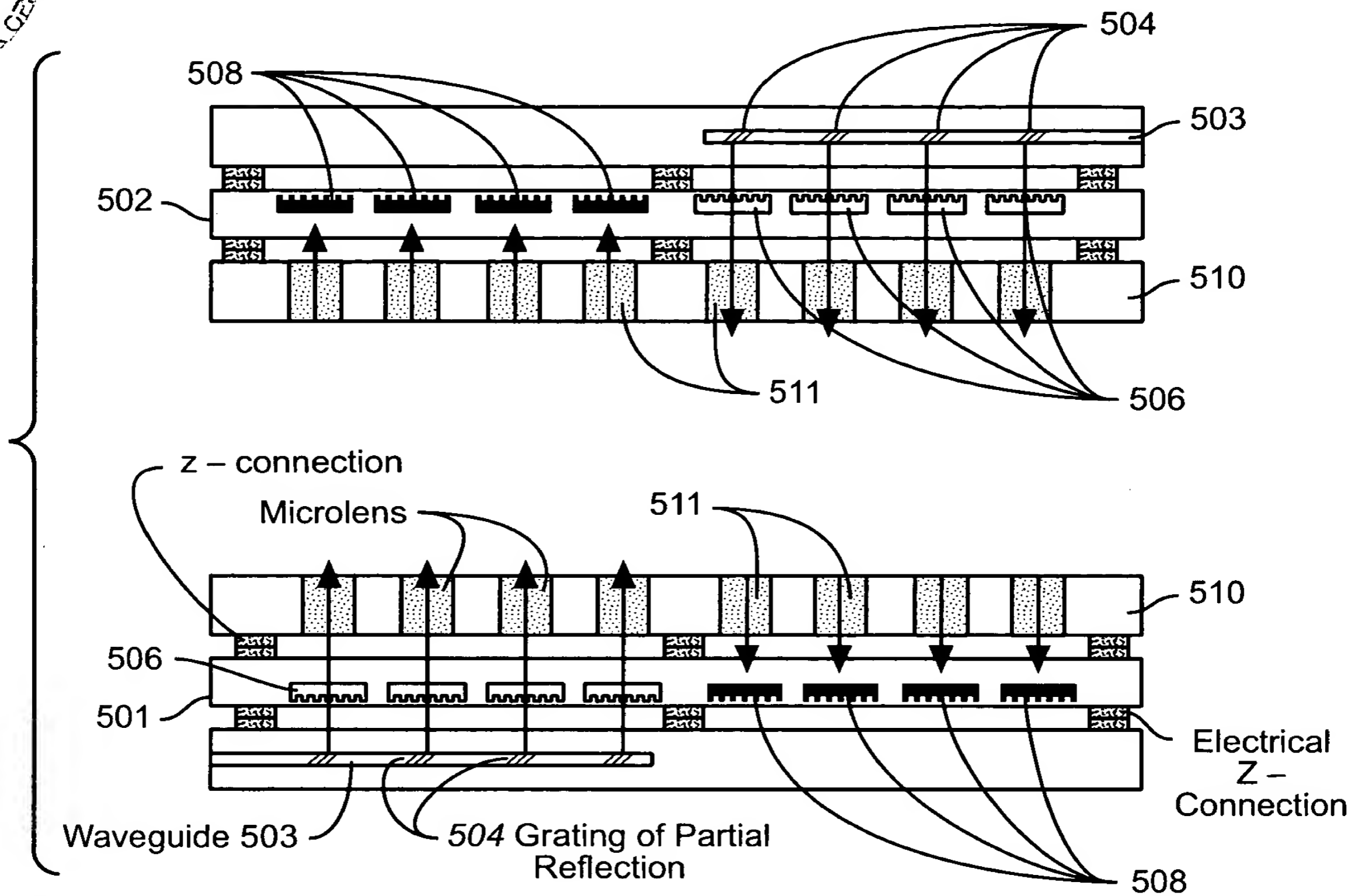
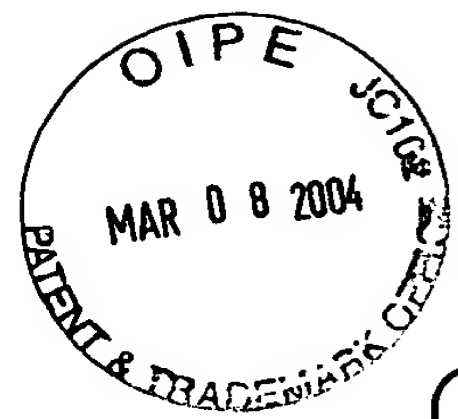


FIG. 69

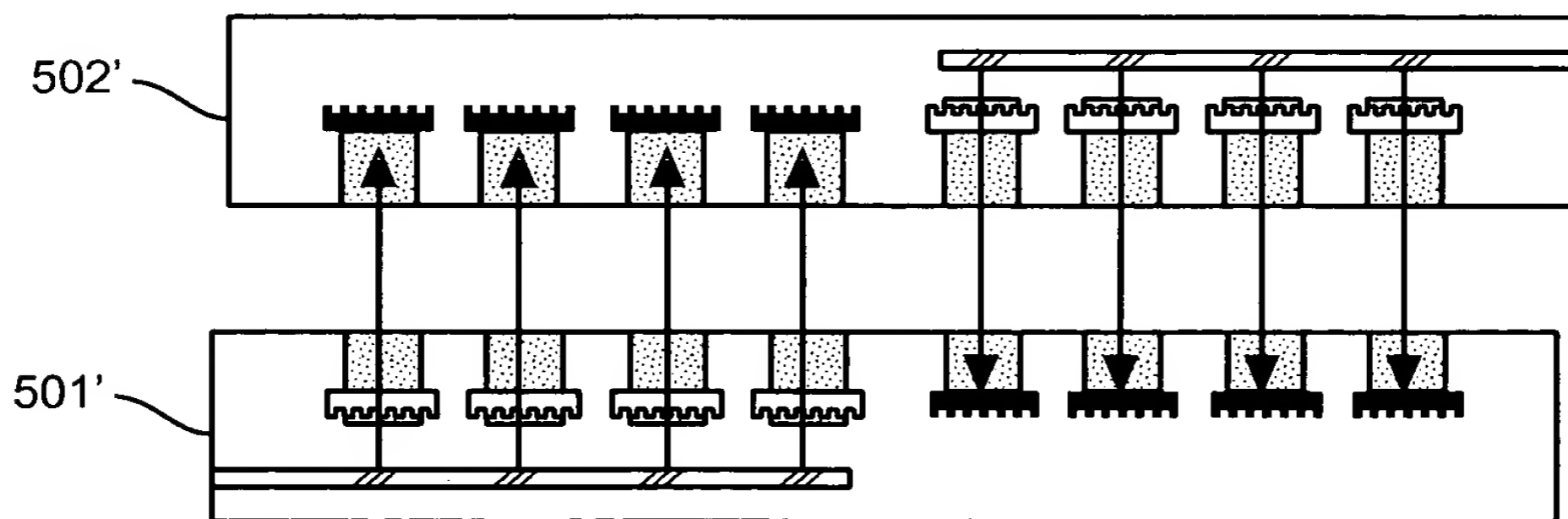


FIG. 70

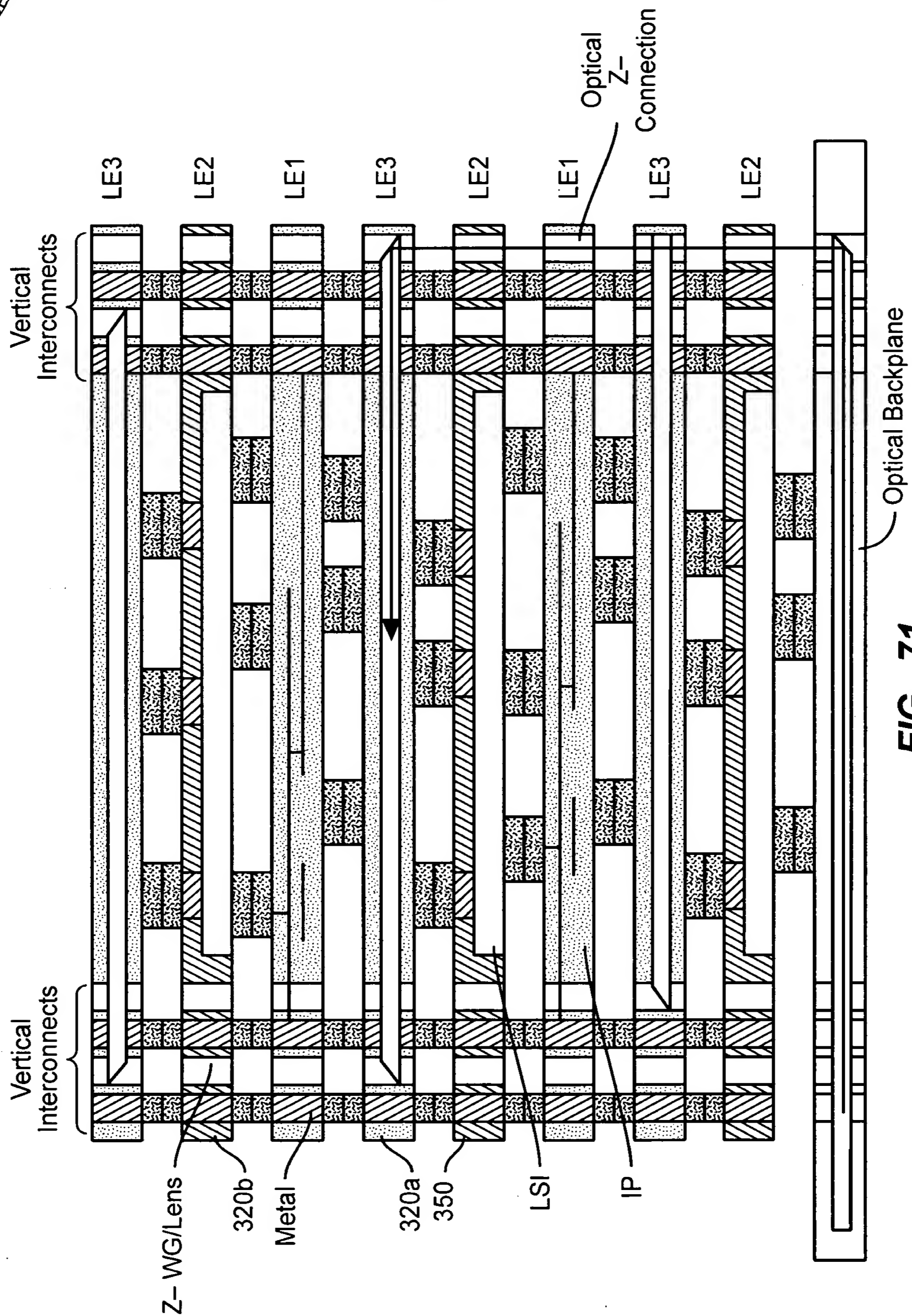
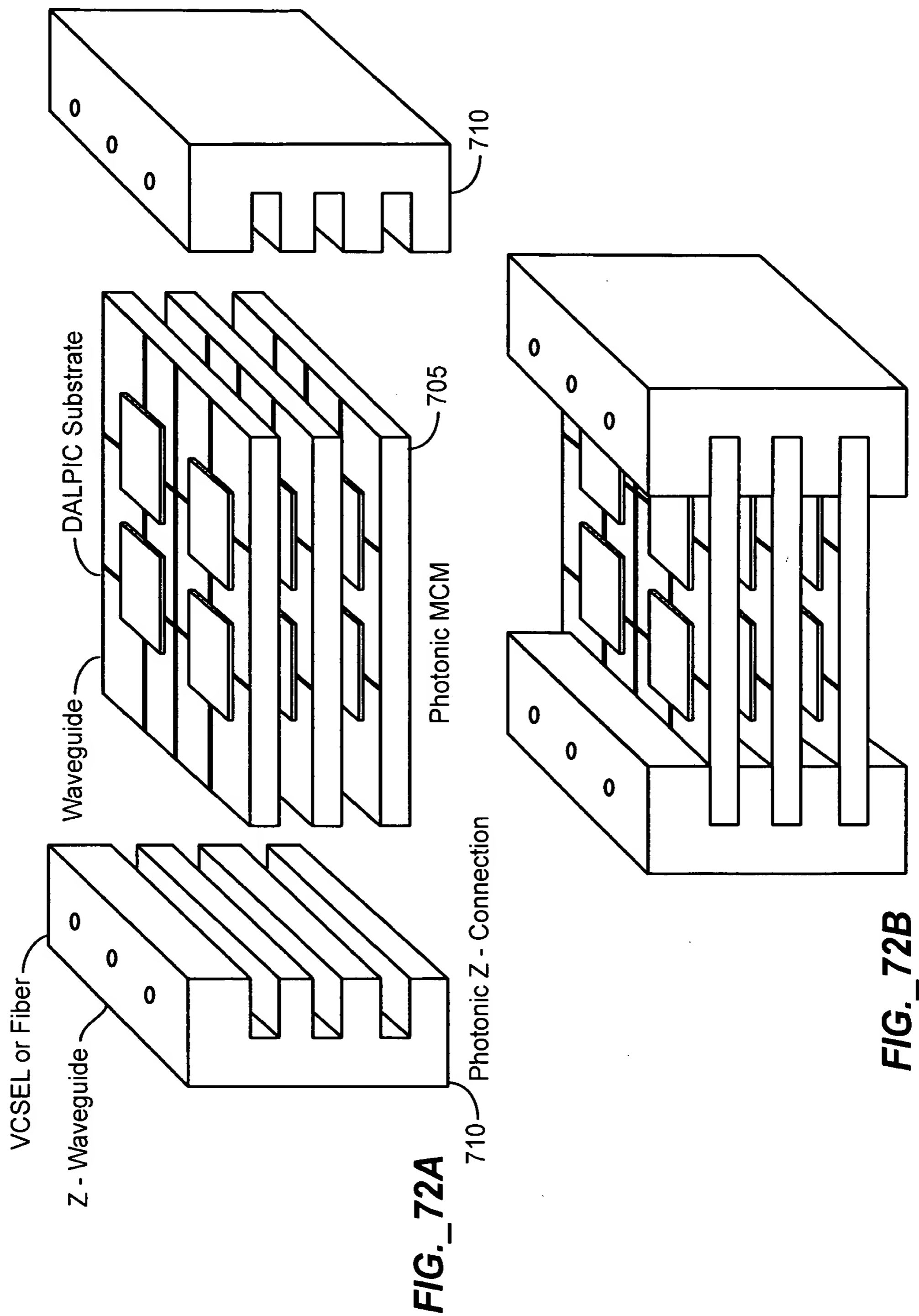


FIG. 71



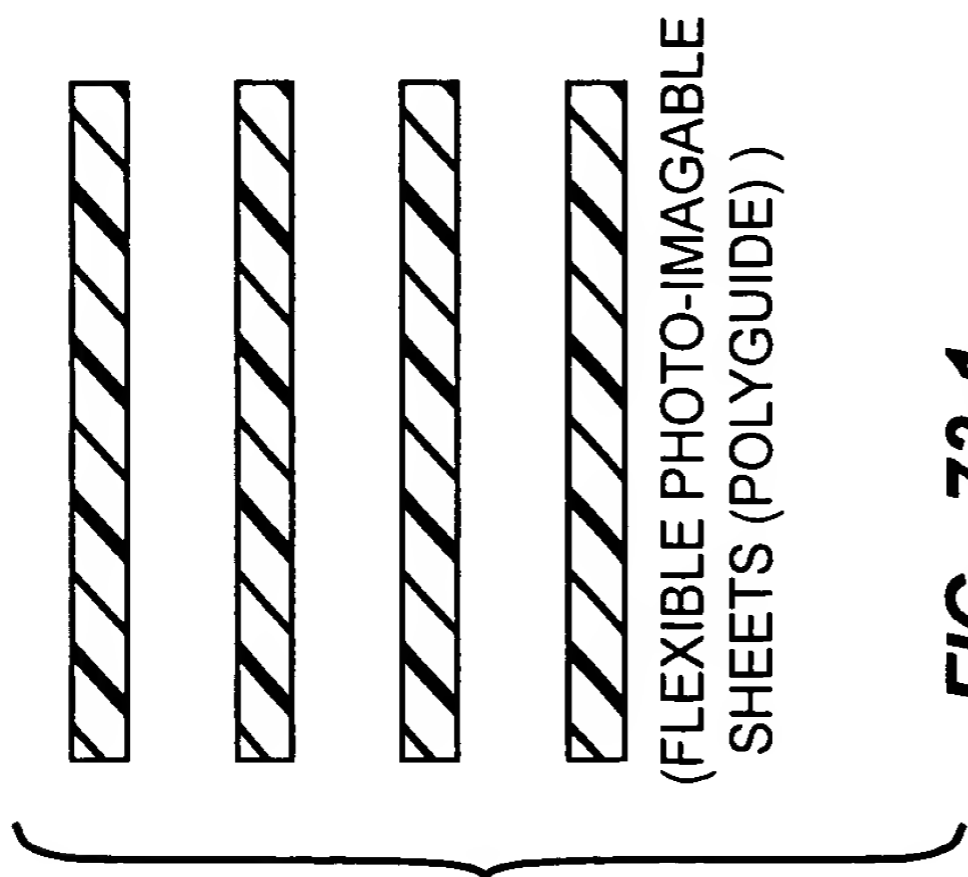


FIG. 73-1

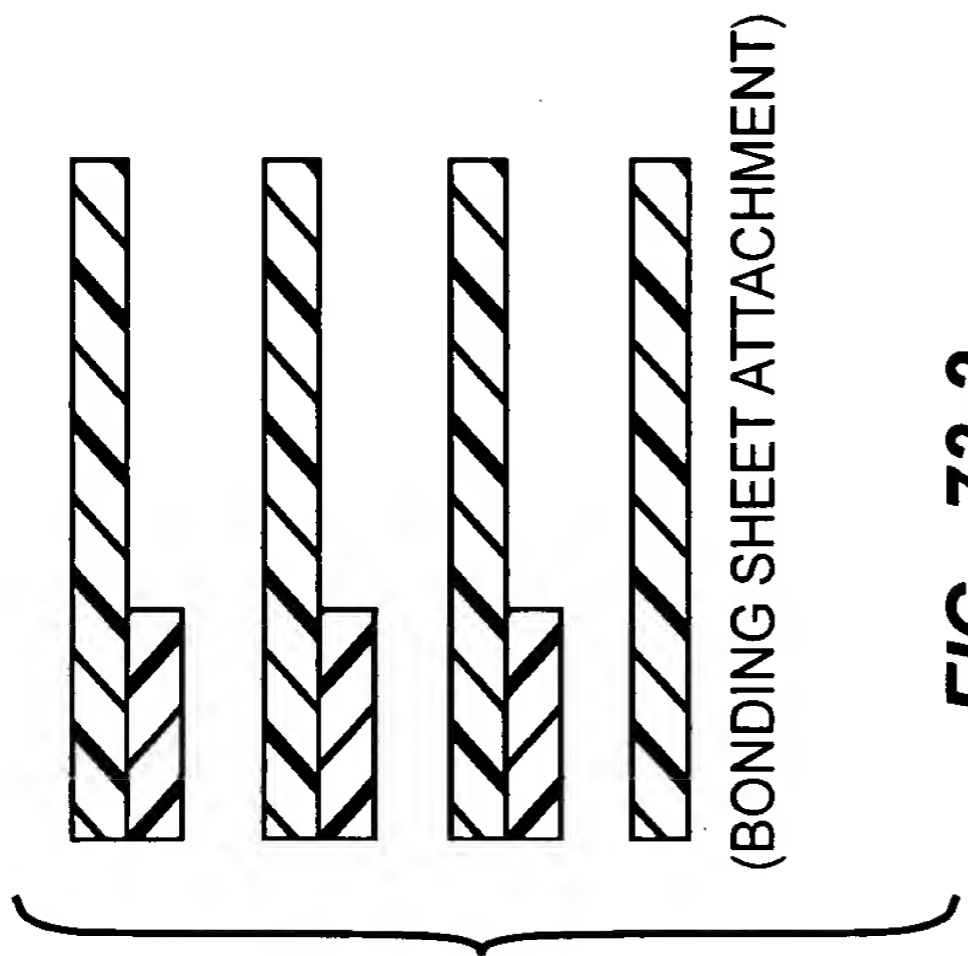


FIG. 73-2

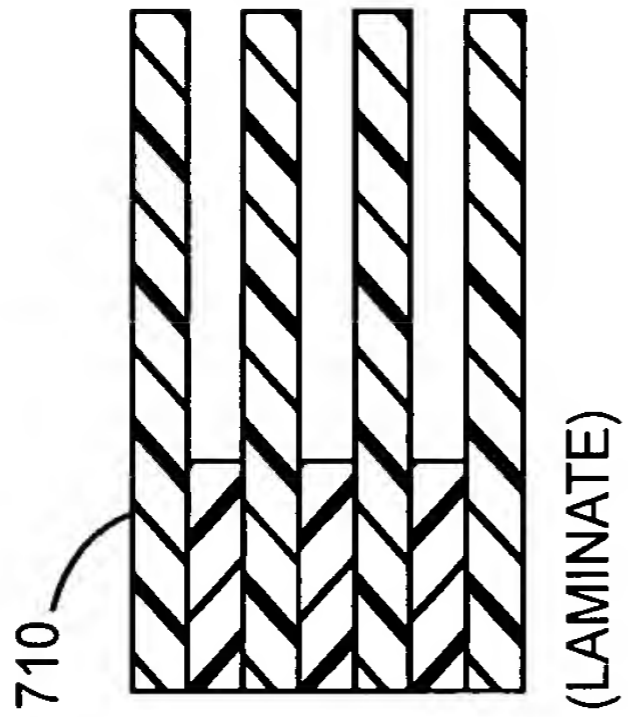


FIG. 73-3

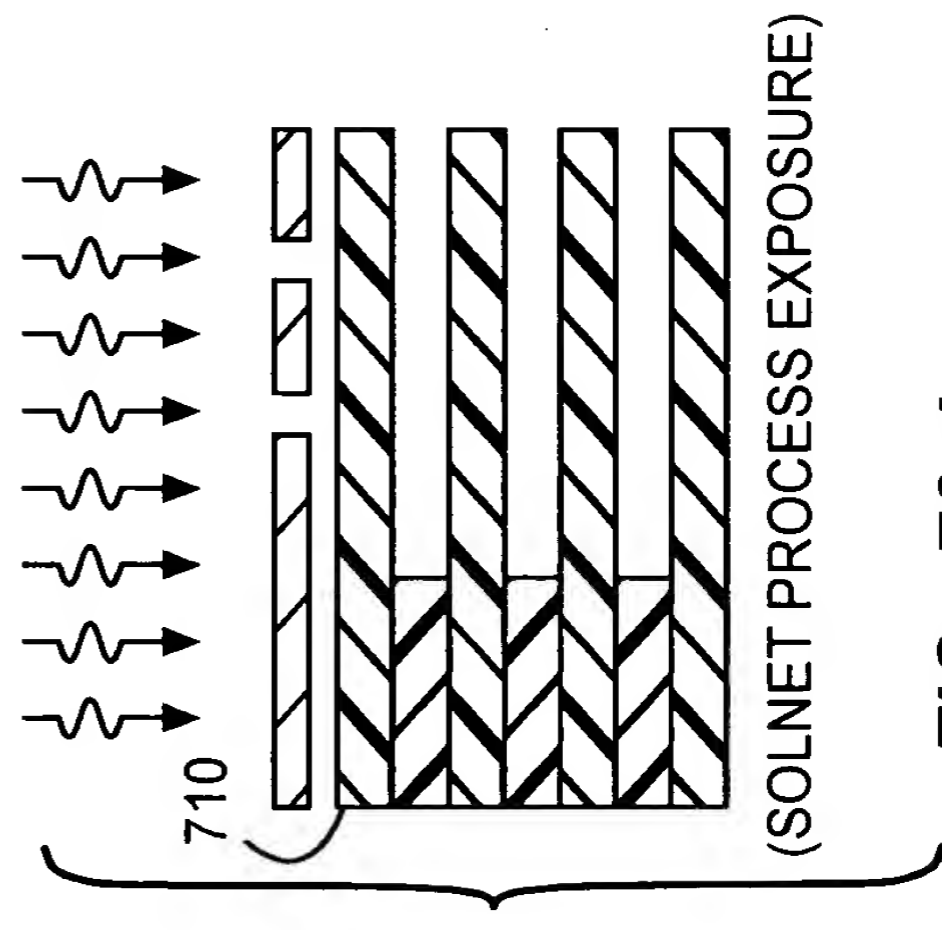


FIG. 73-4

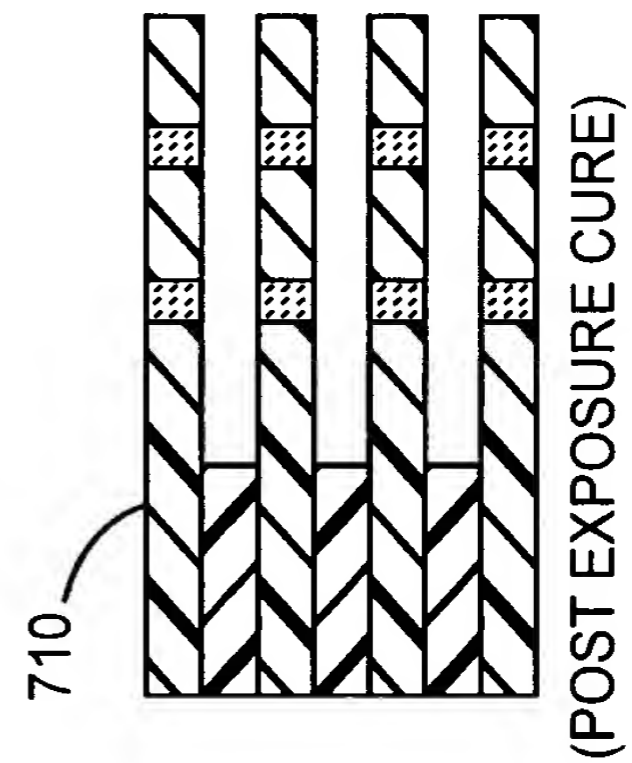


FIG. 73-5

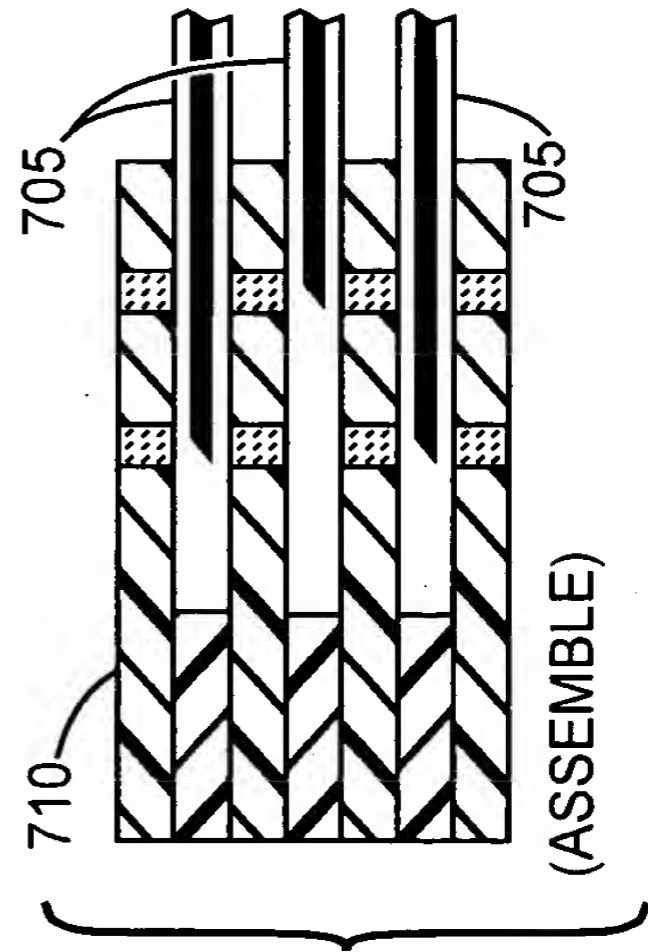


FIG. 73-6

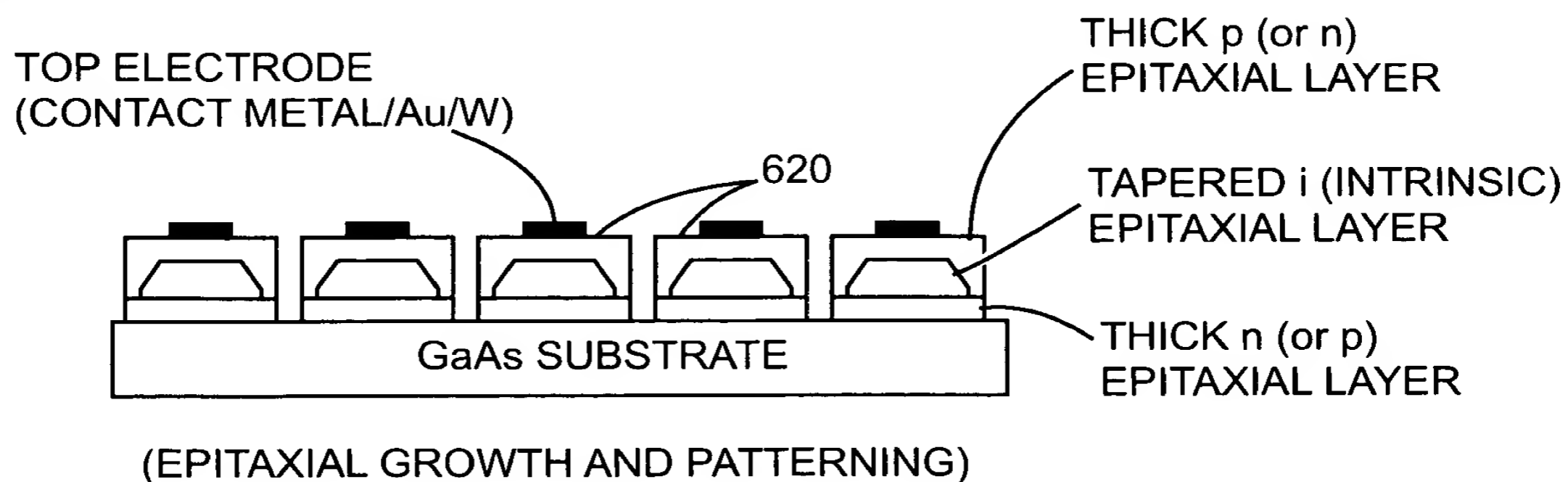


FIG. 74

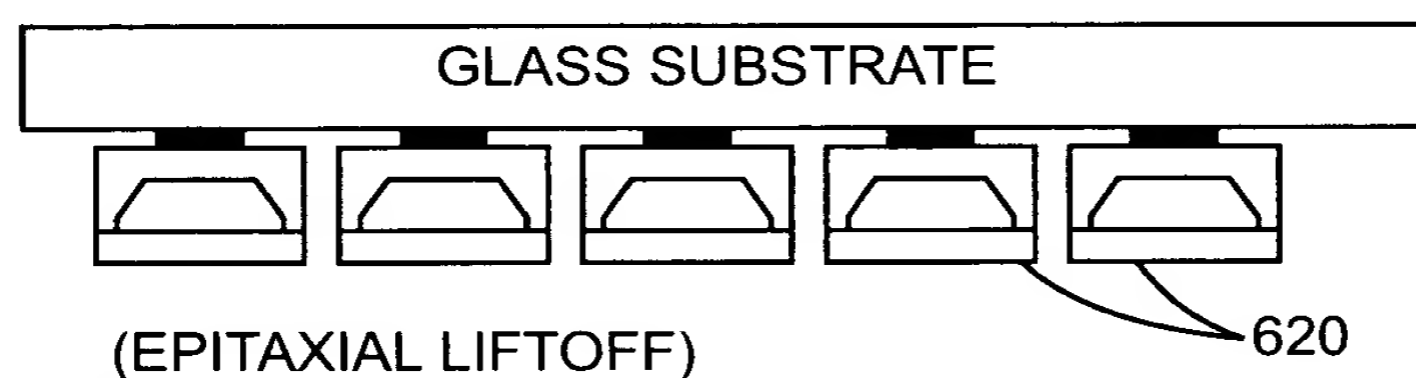


FIG. 75

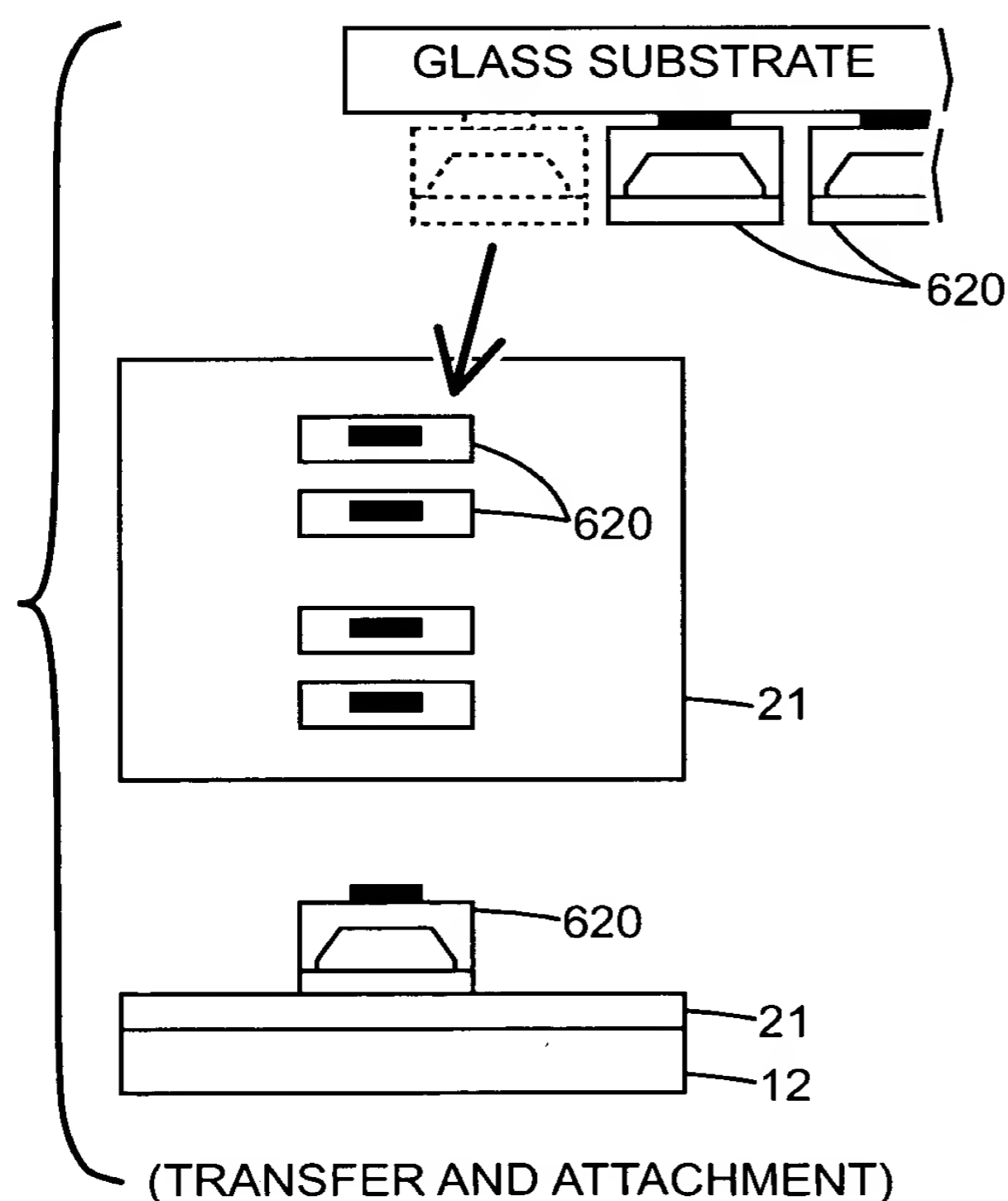


FIG. 76

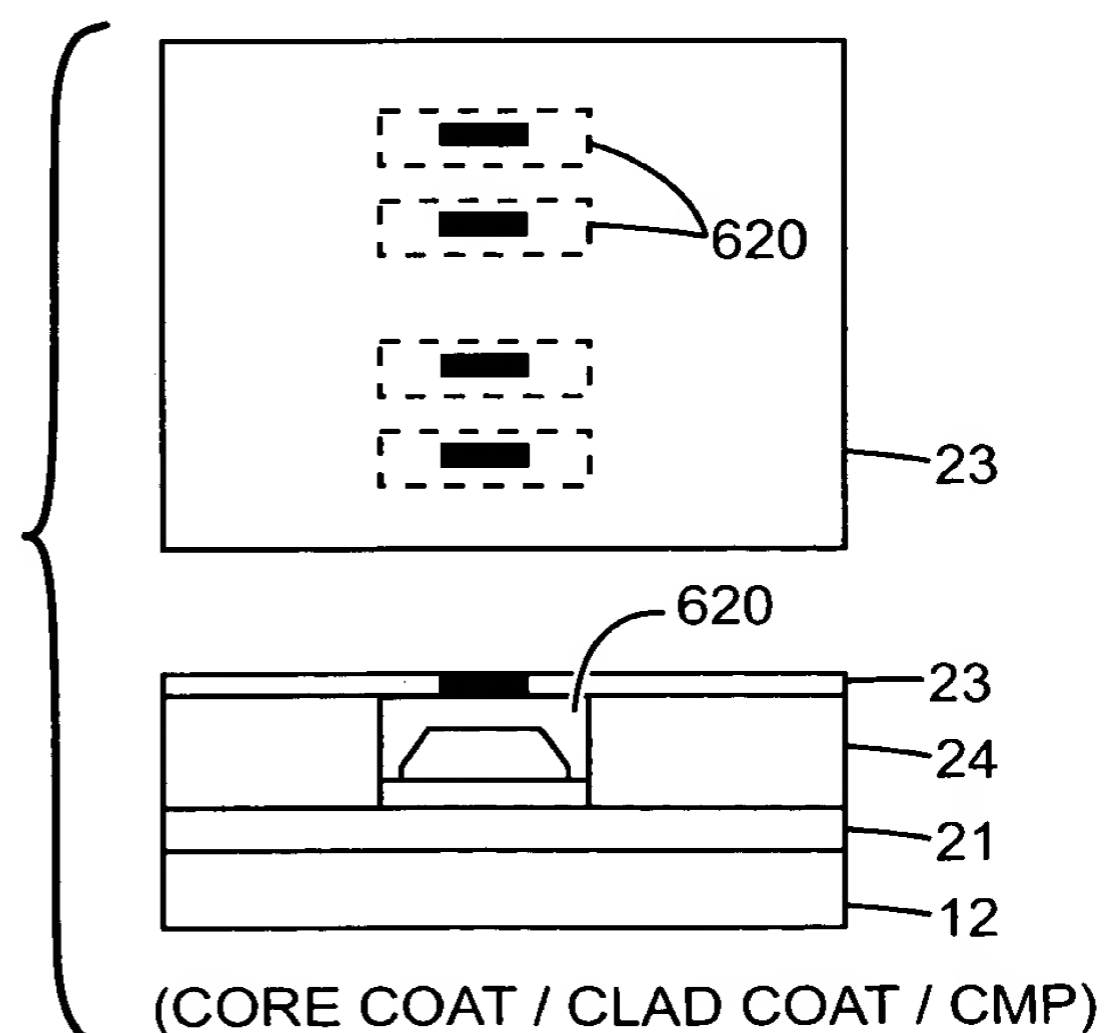


FIG. 77

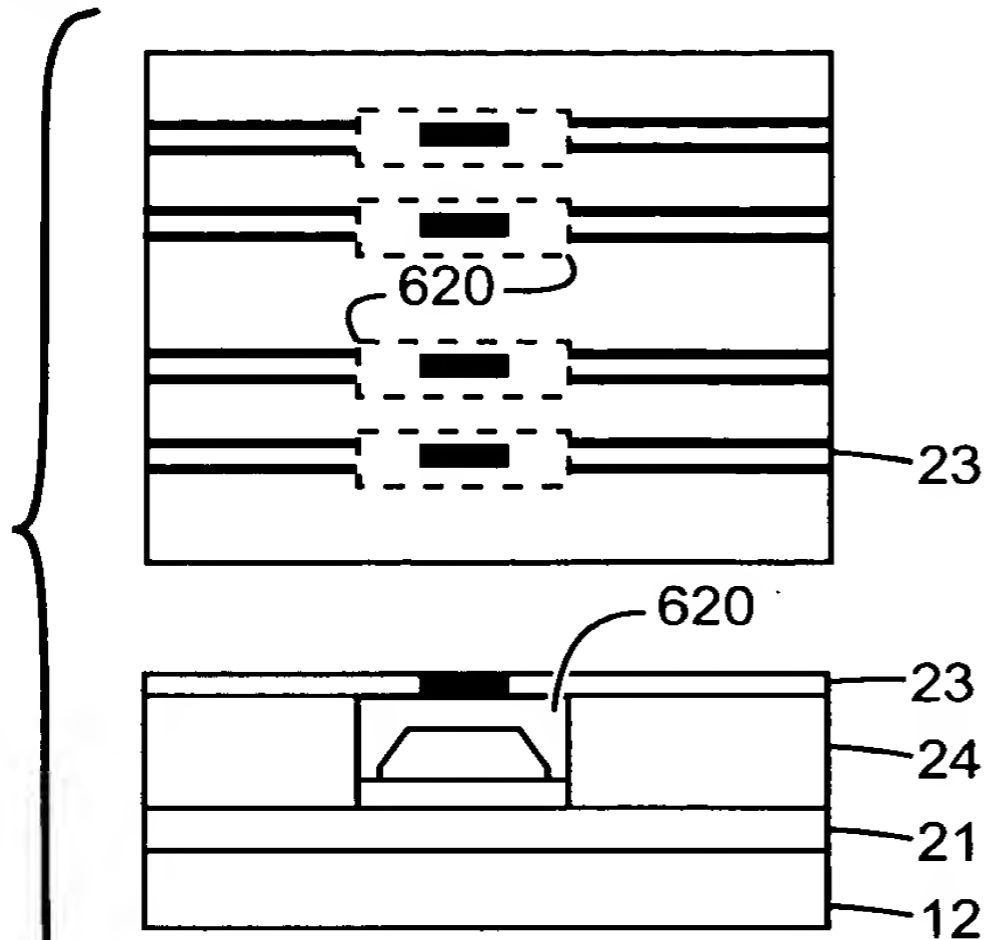


FIG. 78 (CORE PATTERNING)

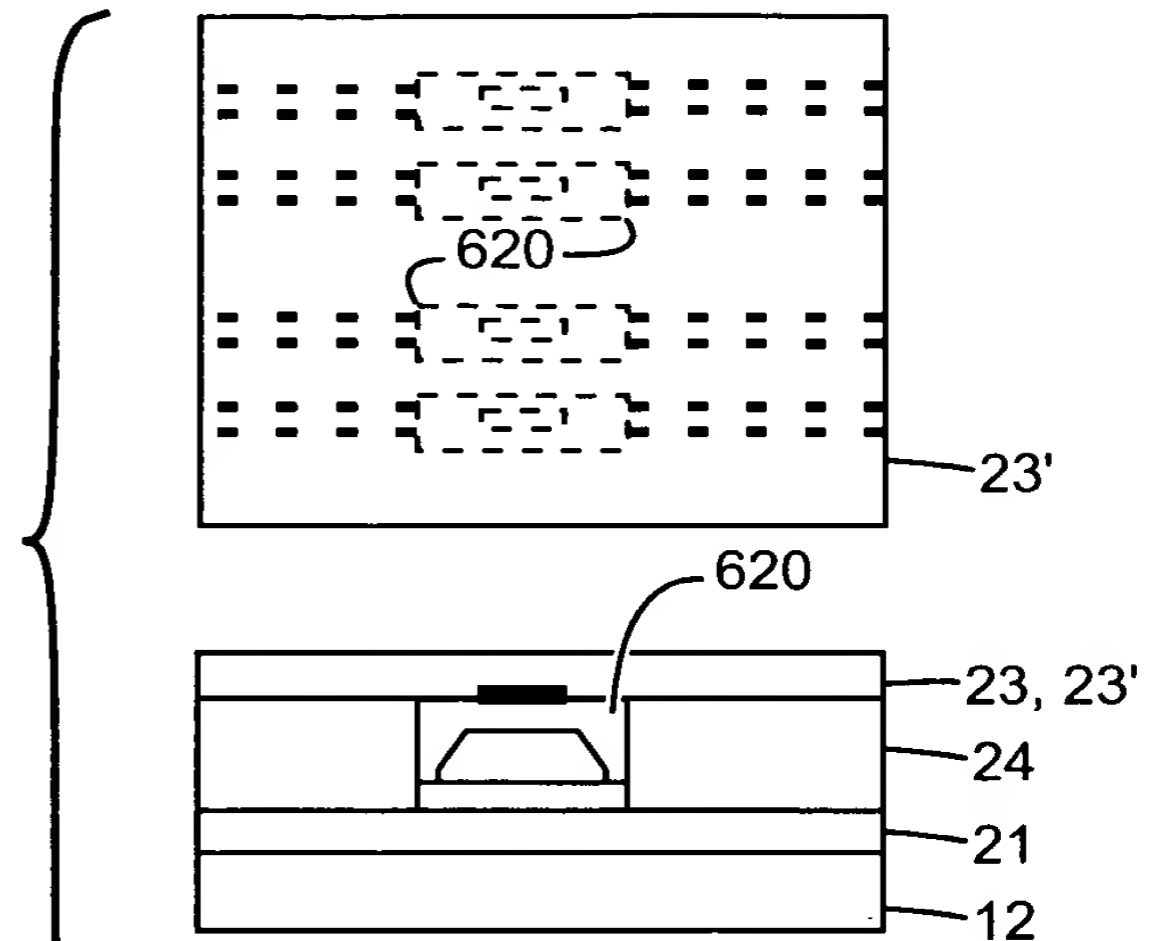
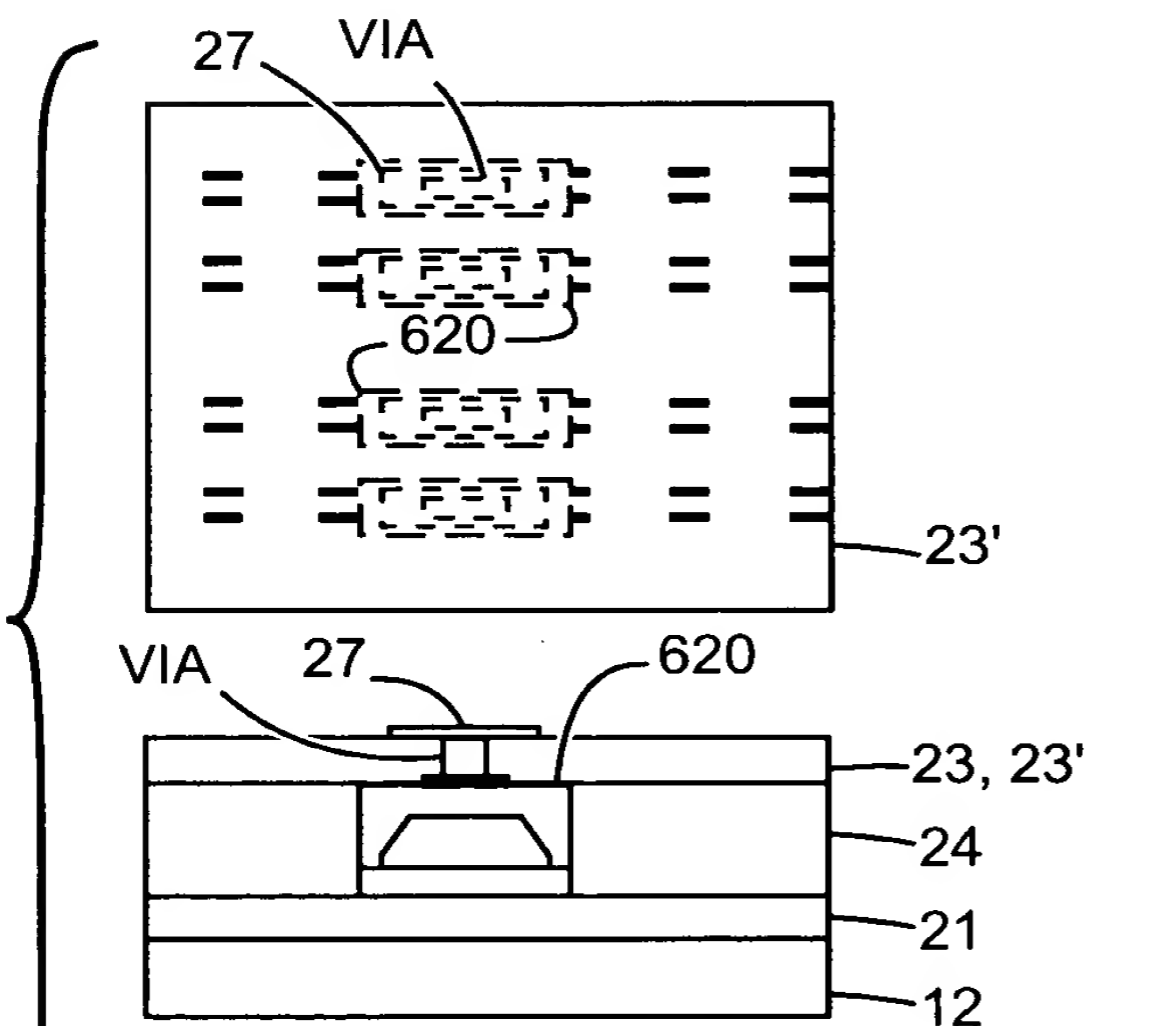
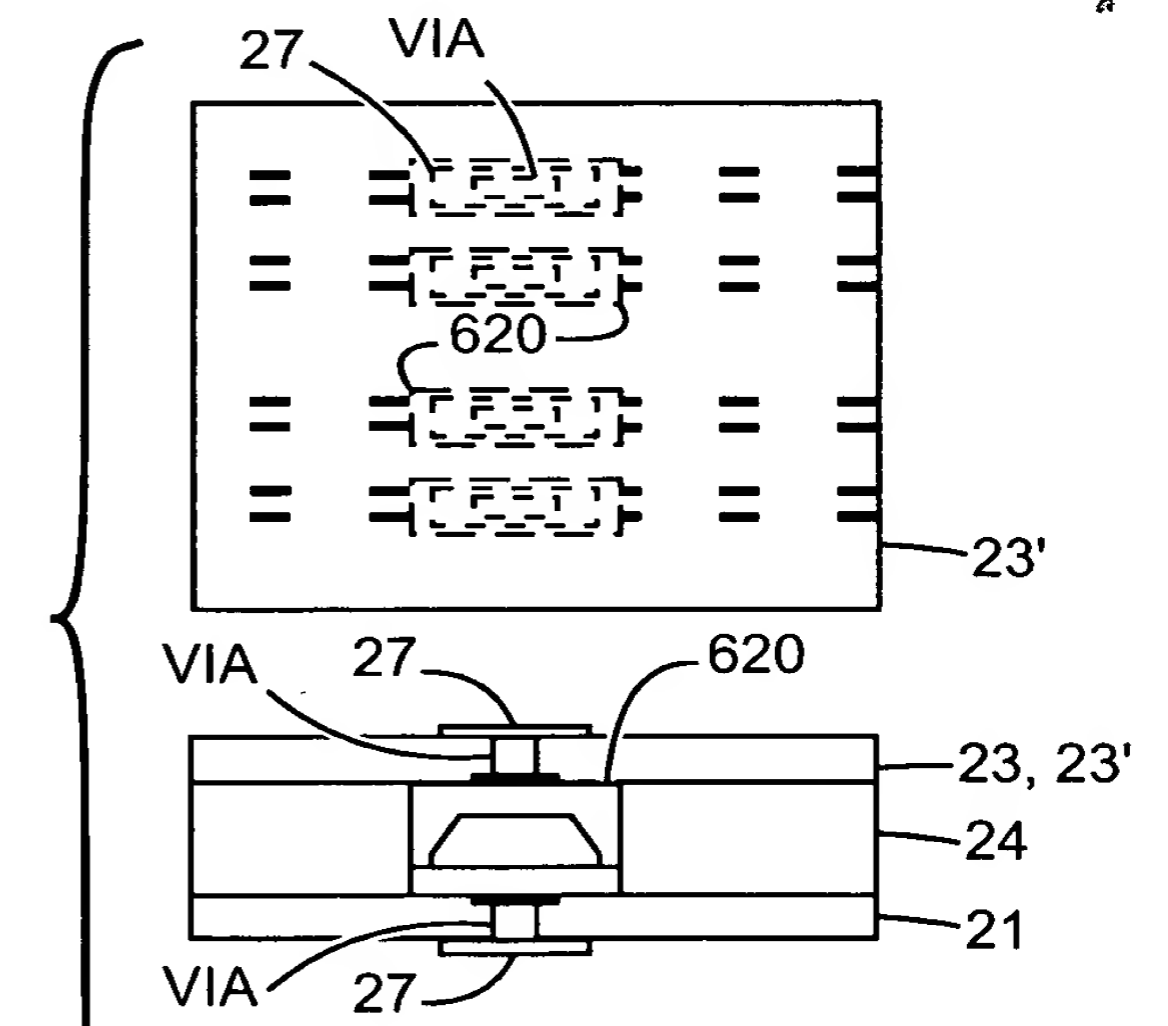


FIG. 79 (CLAD COATING)



(VIA AND ELECTRODE FORMATION)

FIG. 80



(SUBSTRATE REMOVAL /
BACK-SIDE METALIZATION)

FIG. 81

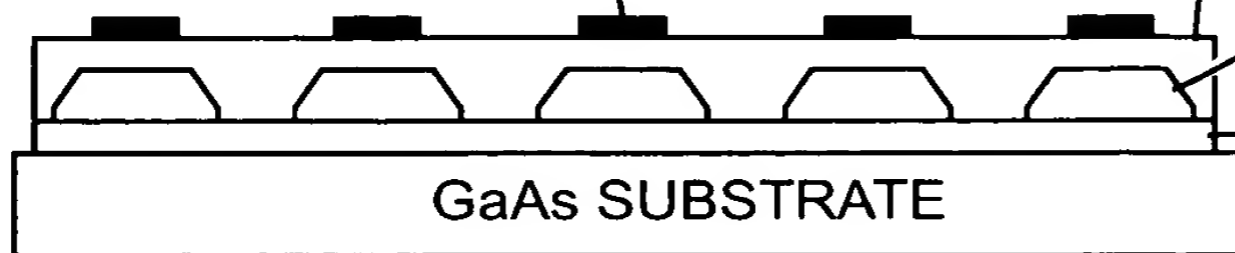


TOP ELECTRODE
(CONTACT METAL/Au/W)

THICK p (or n)
EPITAXIAL LAYER

TAPERED i (INTRINSIC)
EPITAXIAL LAYER (~CORE)

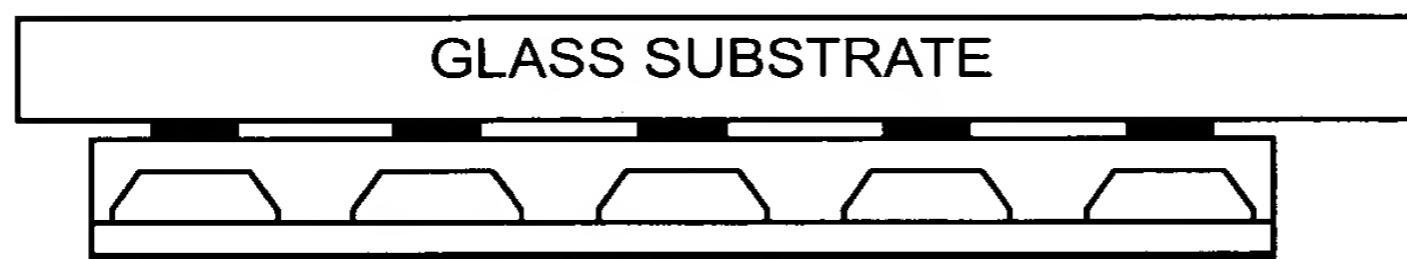
THICK n (or p)
EPITAXIAL LAYER



GaAs SUBSTRATE

FIG. 82

(EPITAXIAL GROWTH)



GLASS SUBSTRATE

FIG. 83

METALIZATION

(EPITAXIAL LIFTOFF AND METALIZATION)

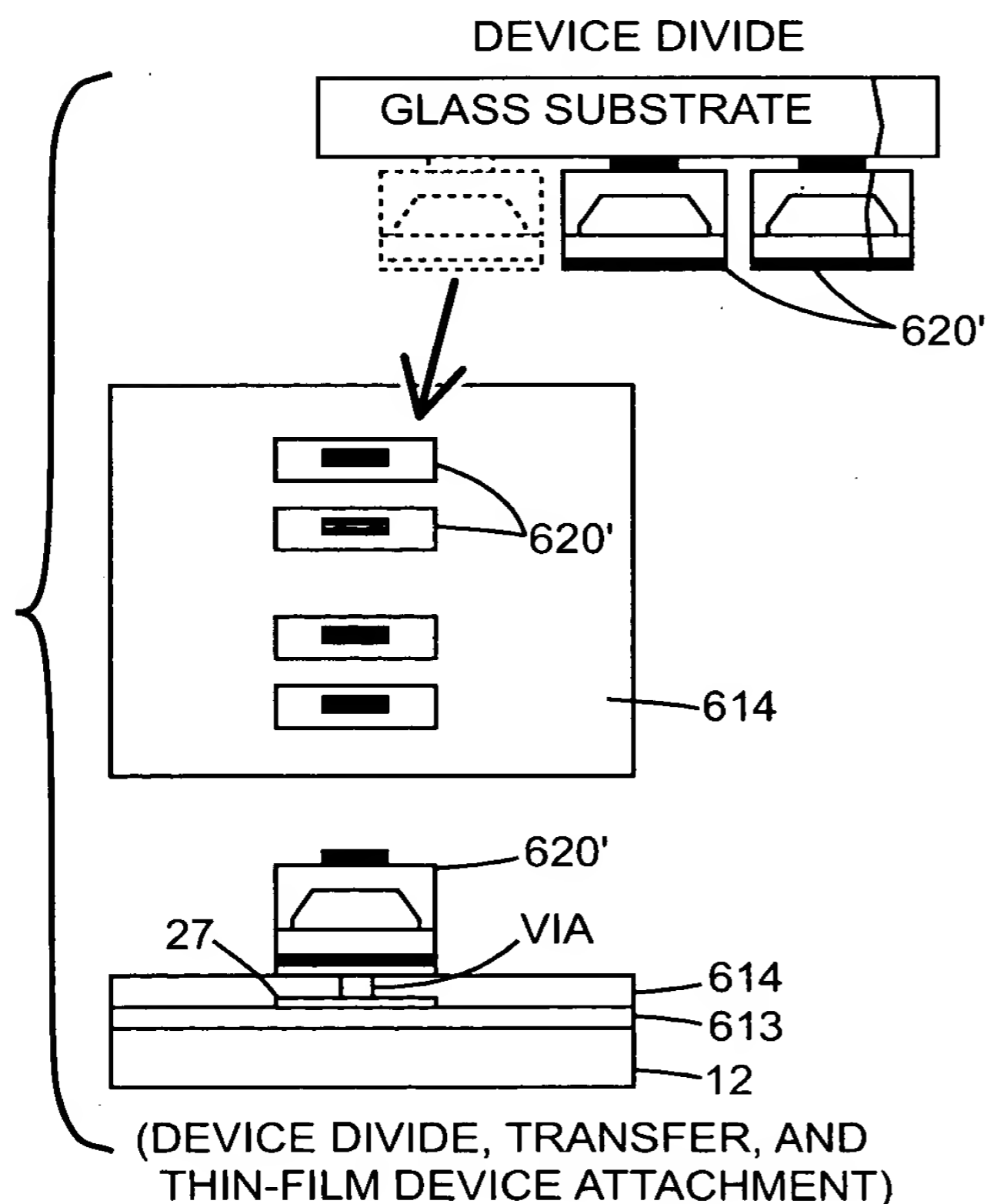


FIG. 84

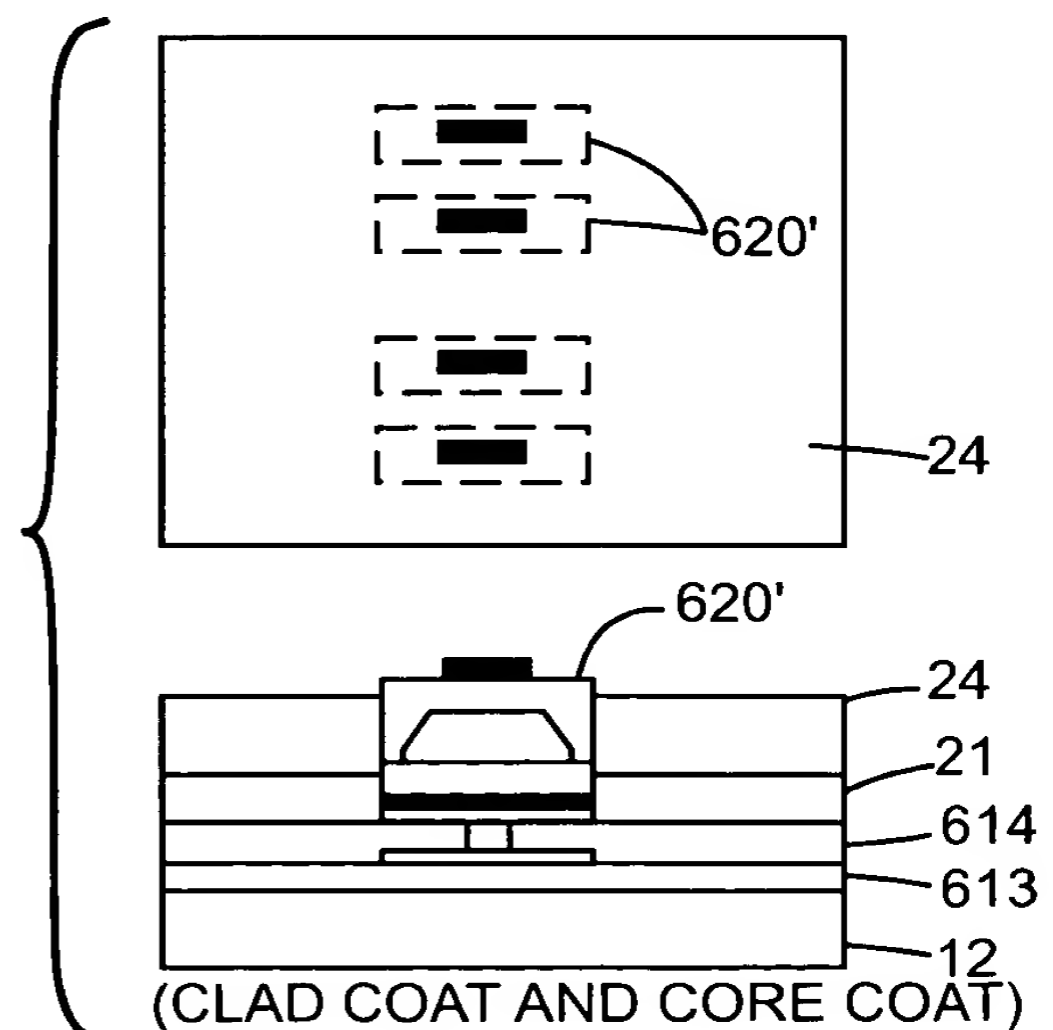


FIG. 85



"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

34 / 61

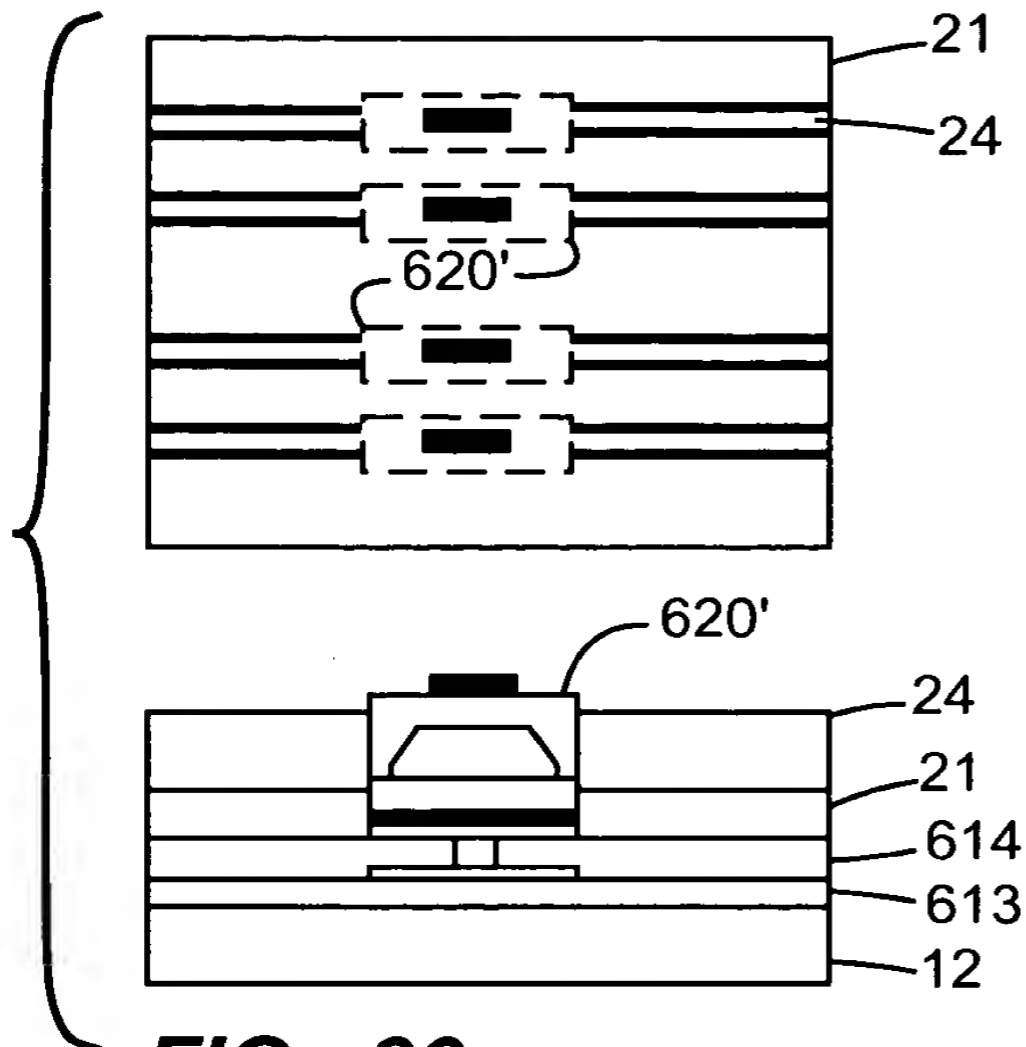


FIG._86 (CORE PATTERNING)

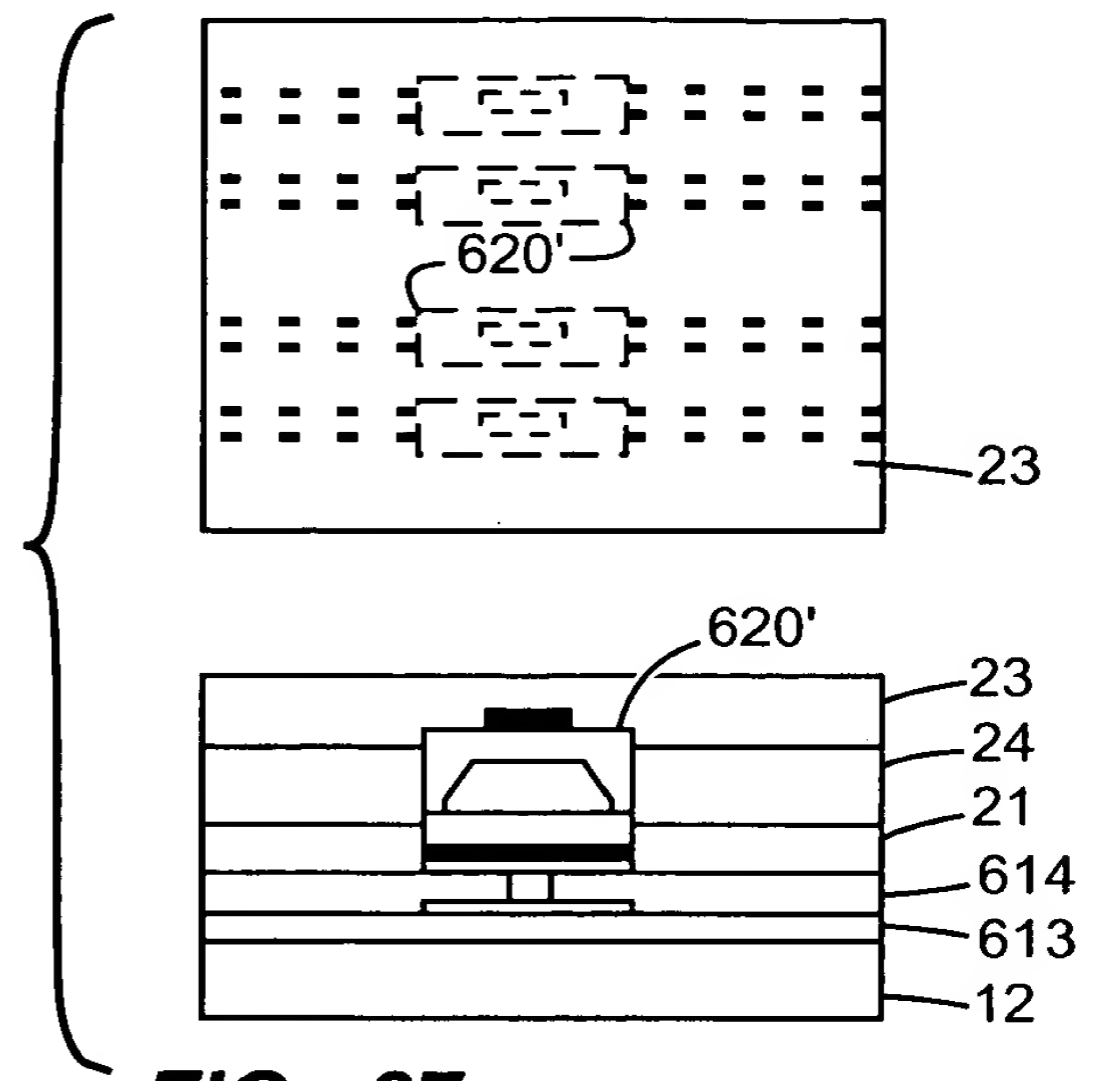


FIG._87 (CLAD COATING)

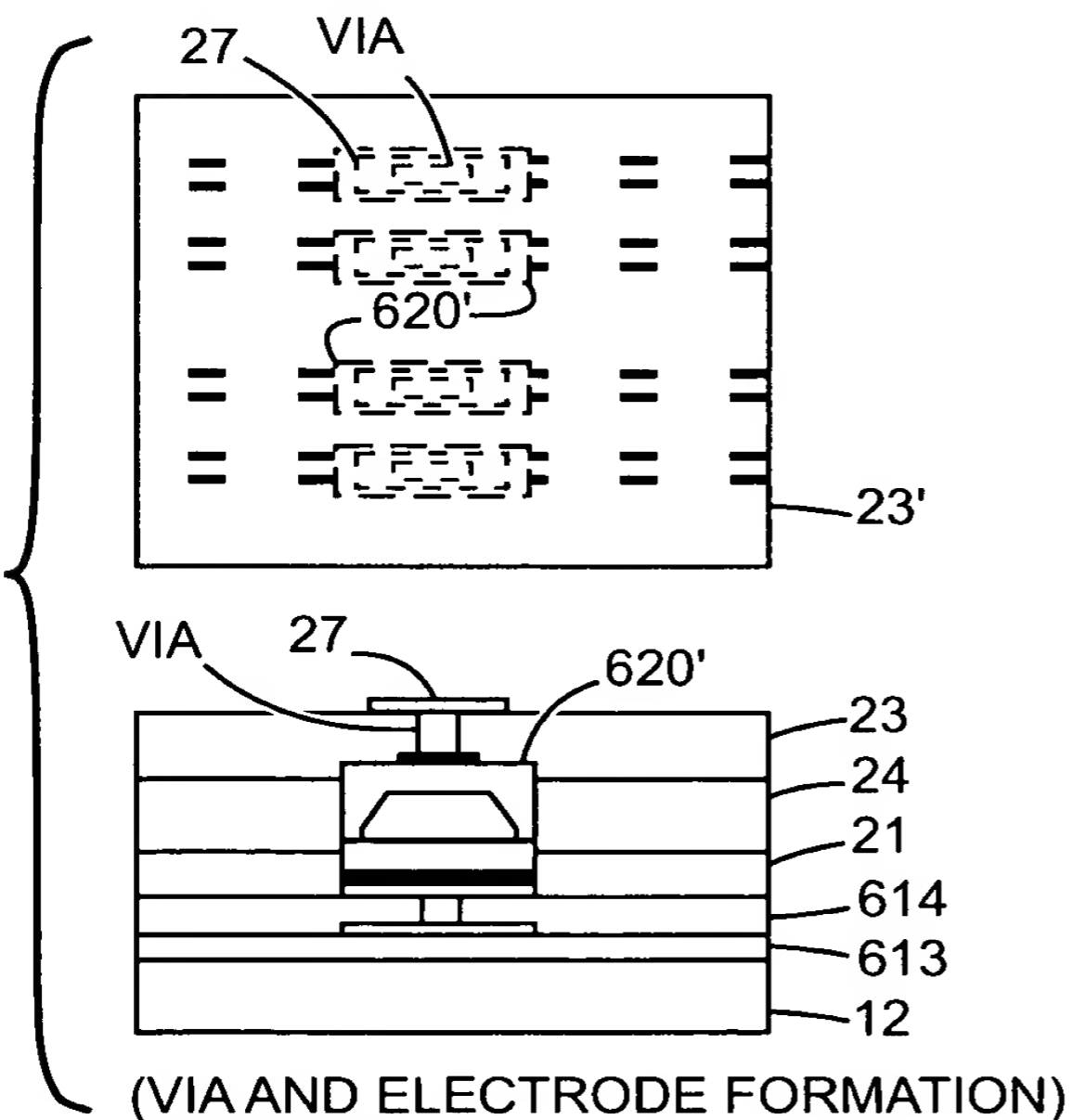


FIG._88

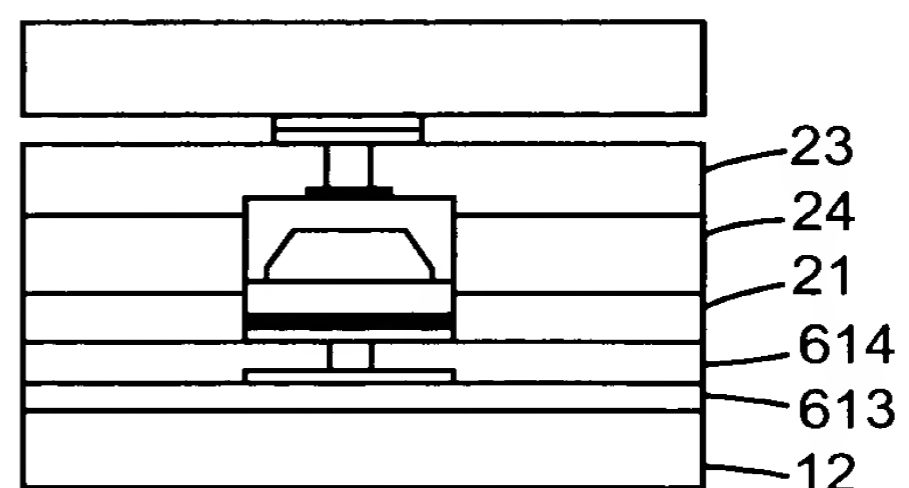
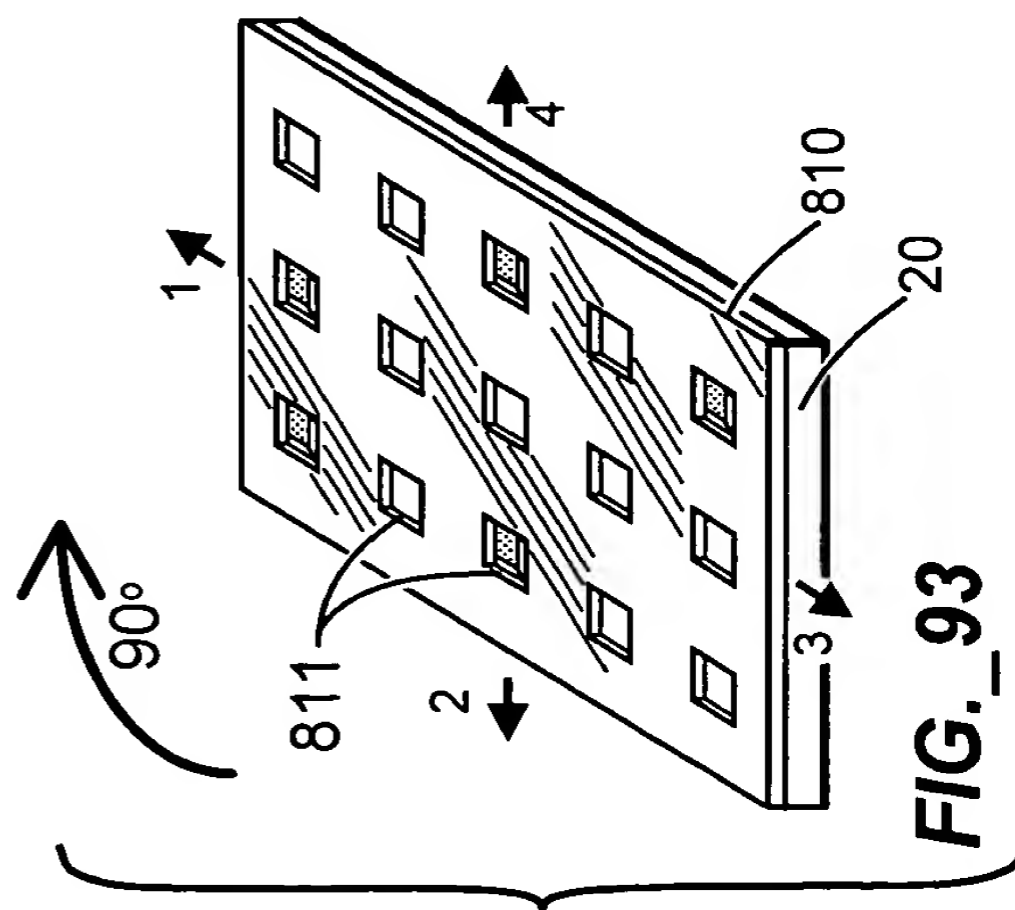
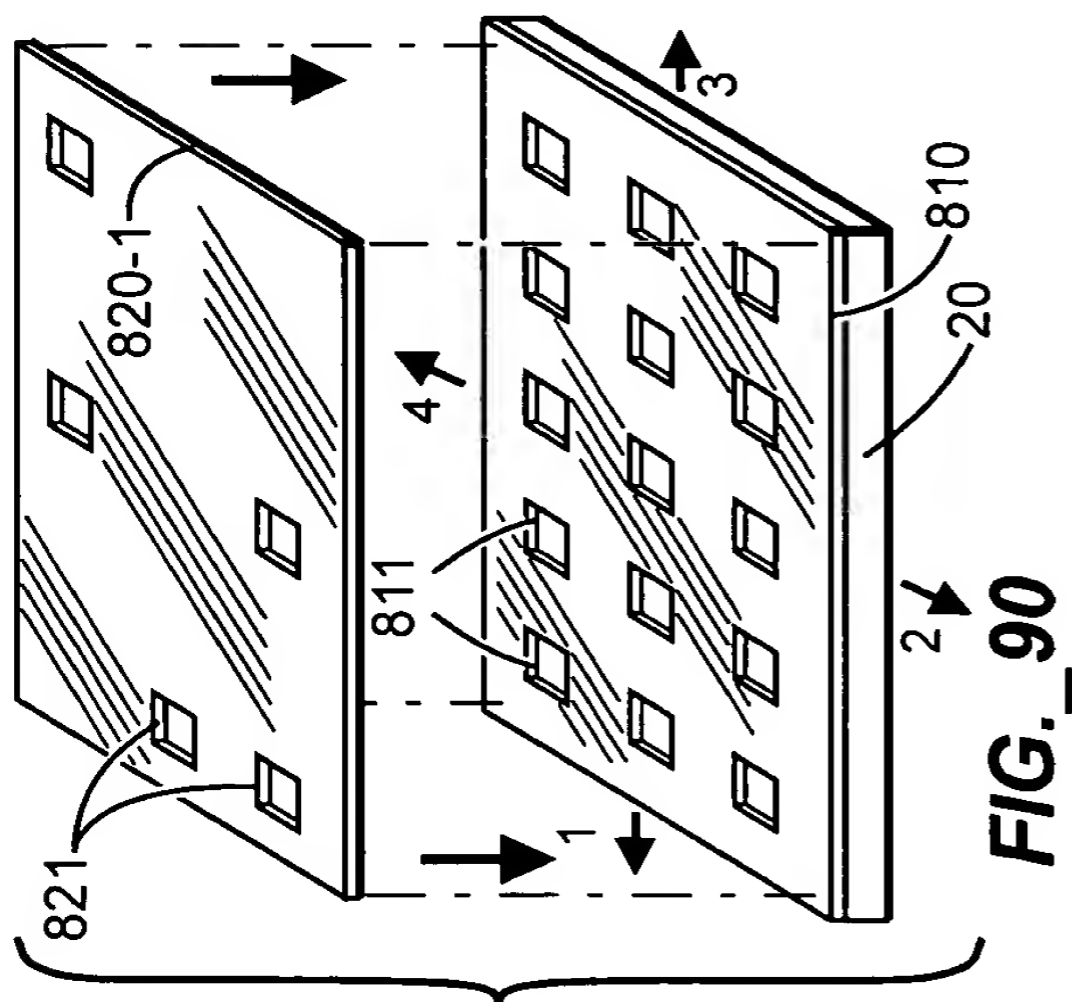
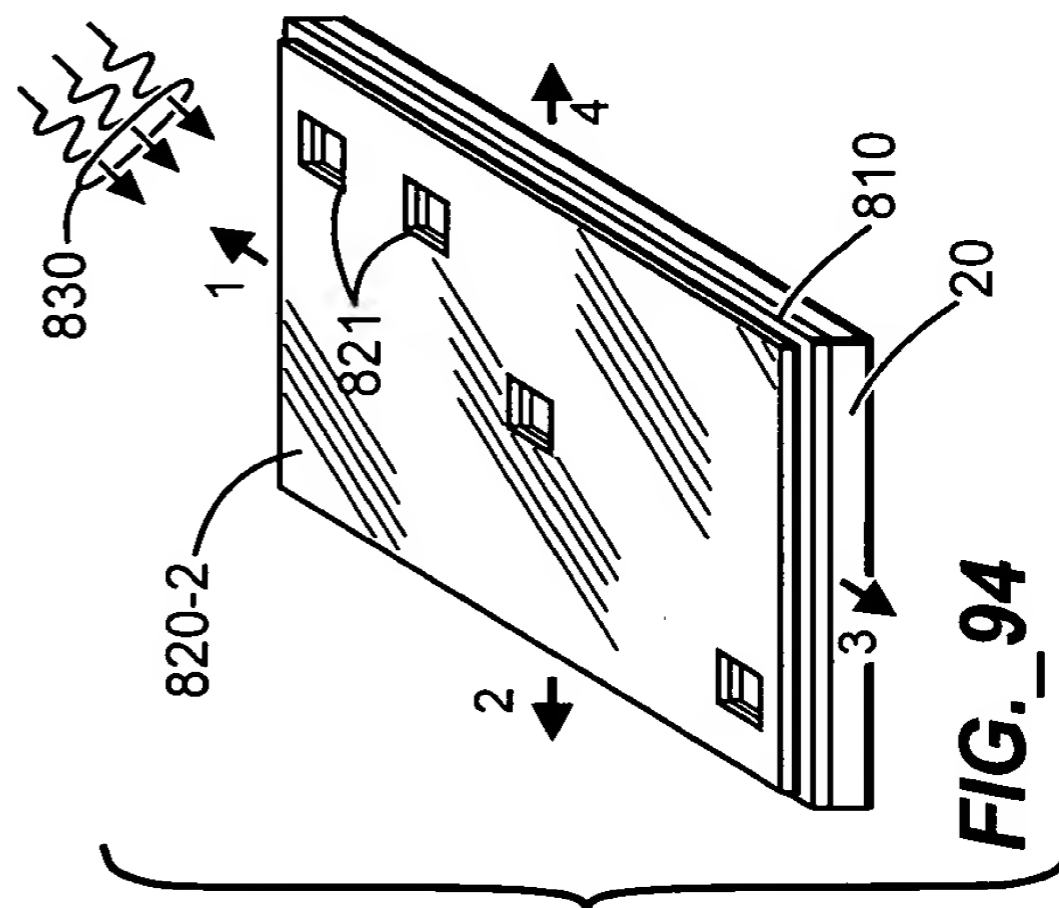
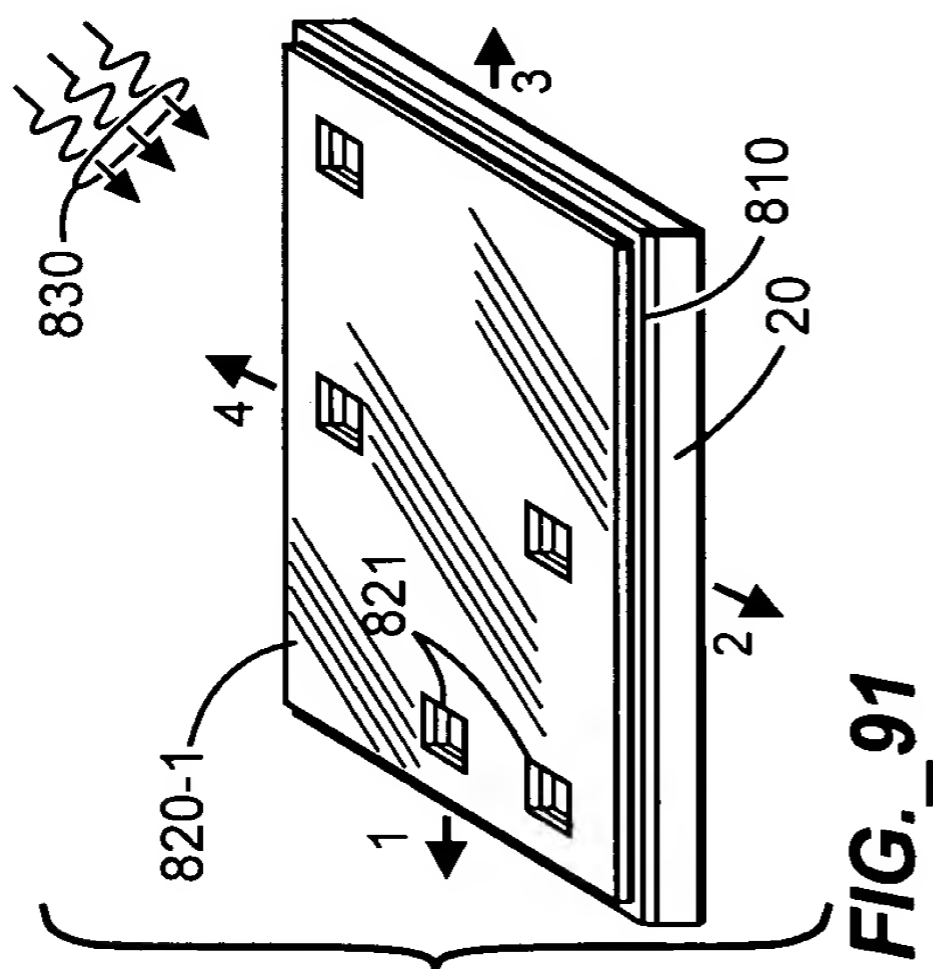
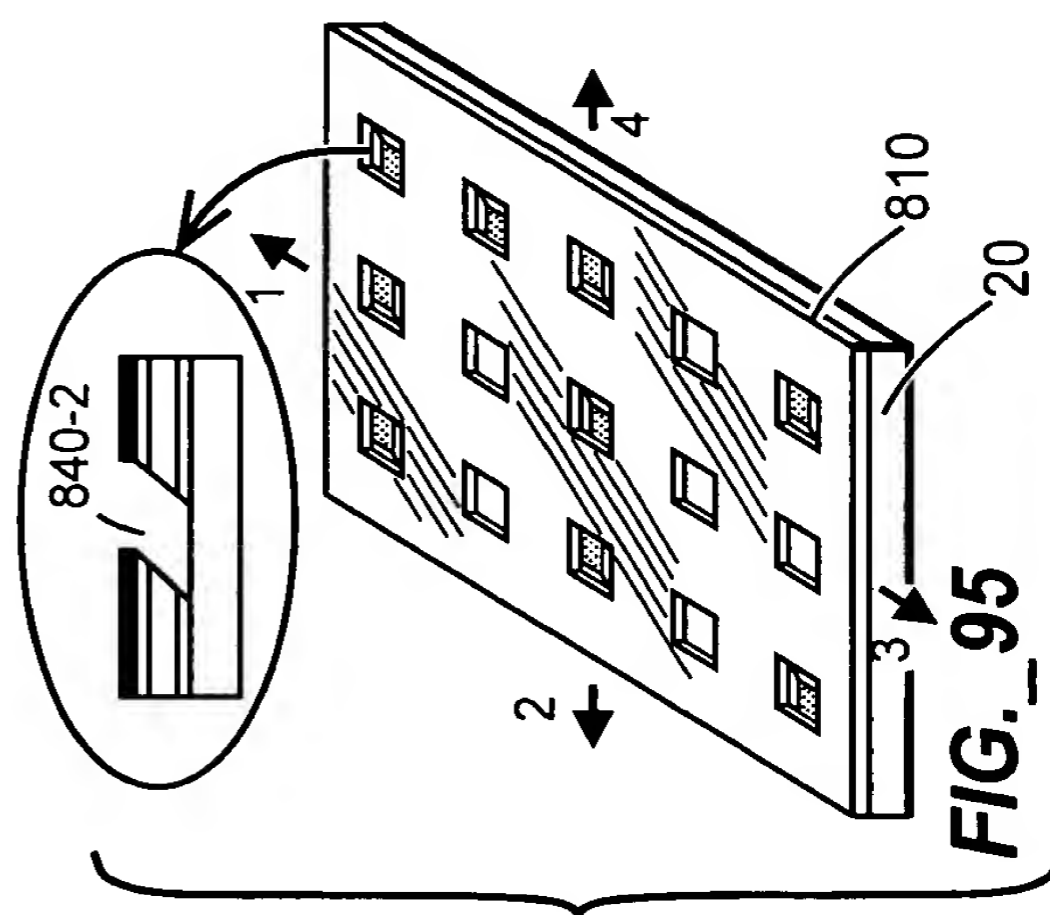
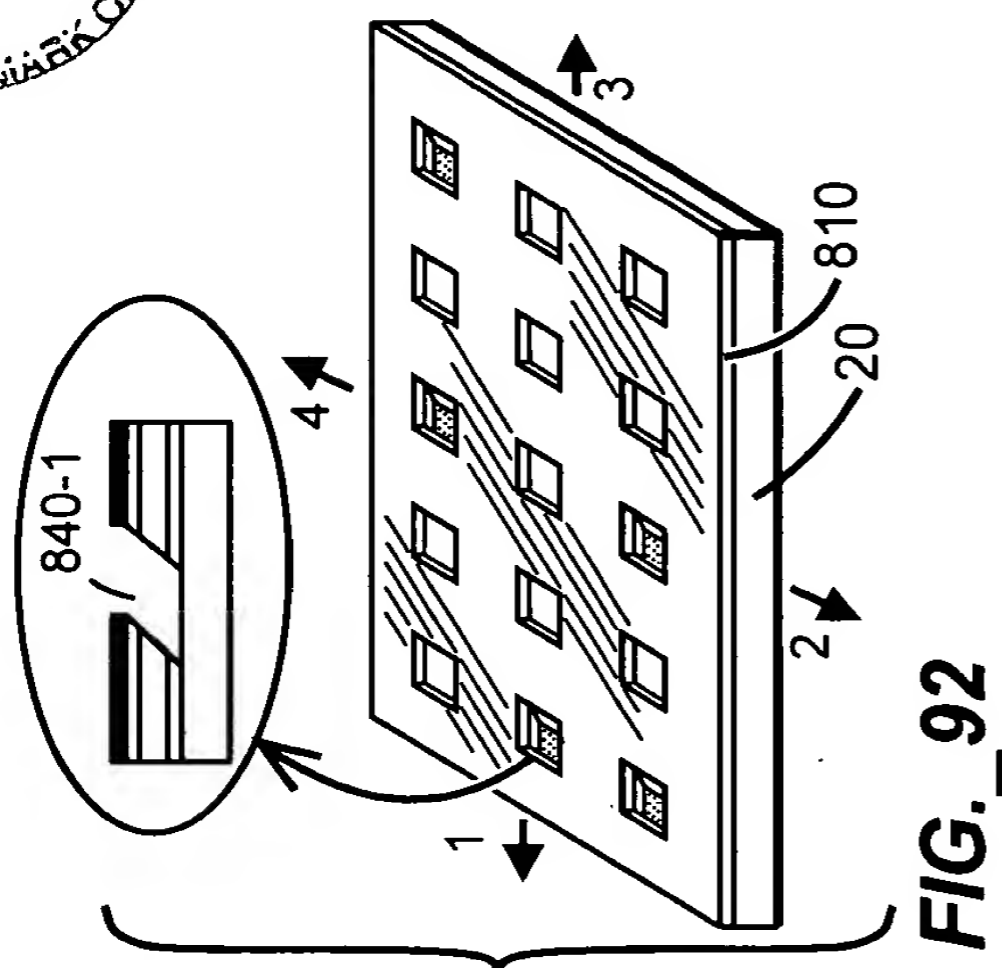
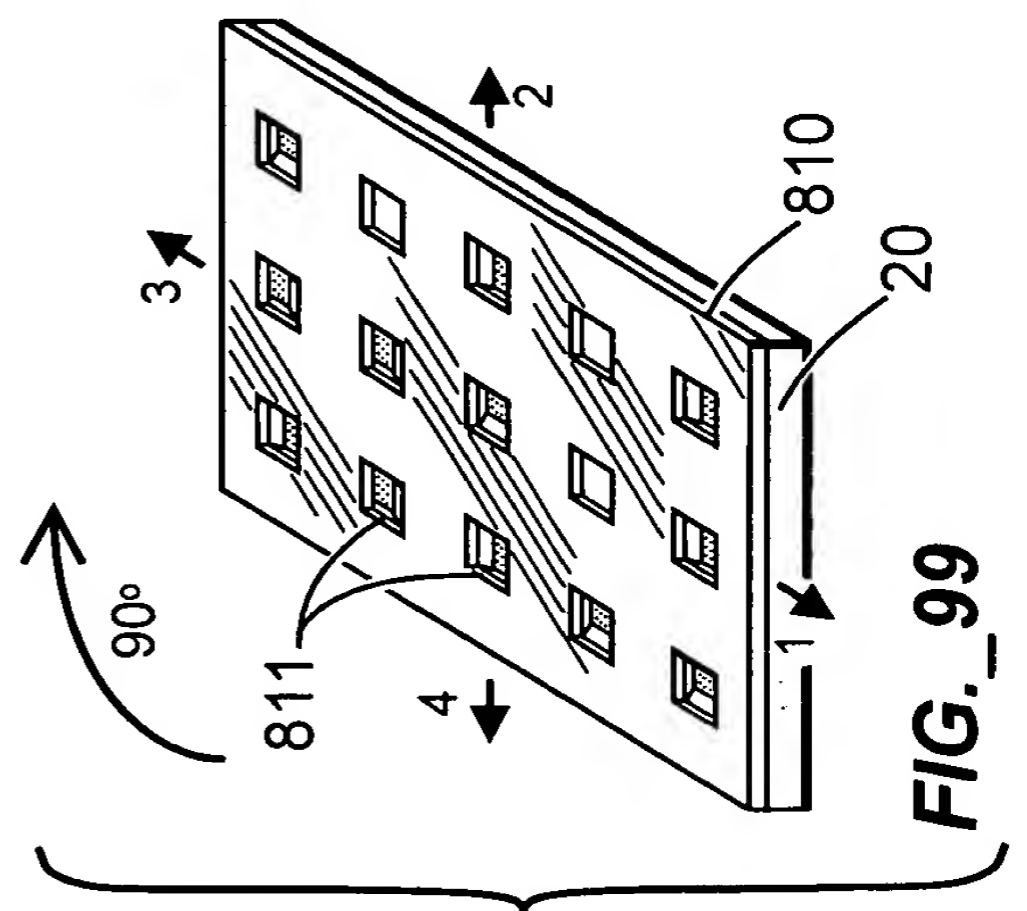
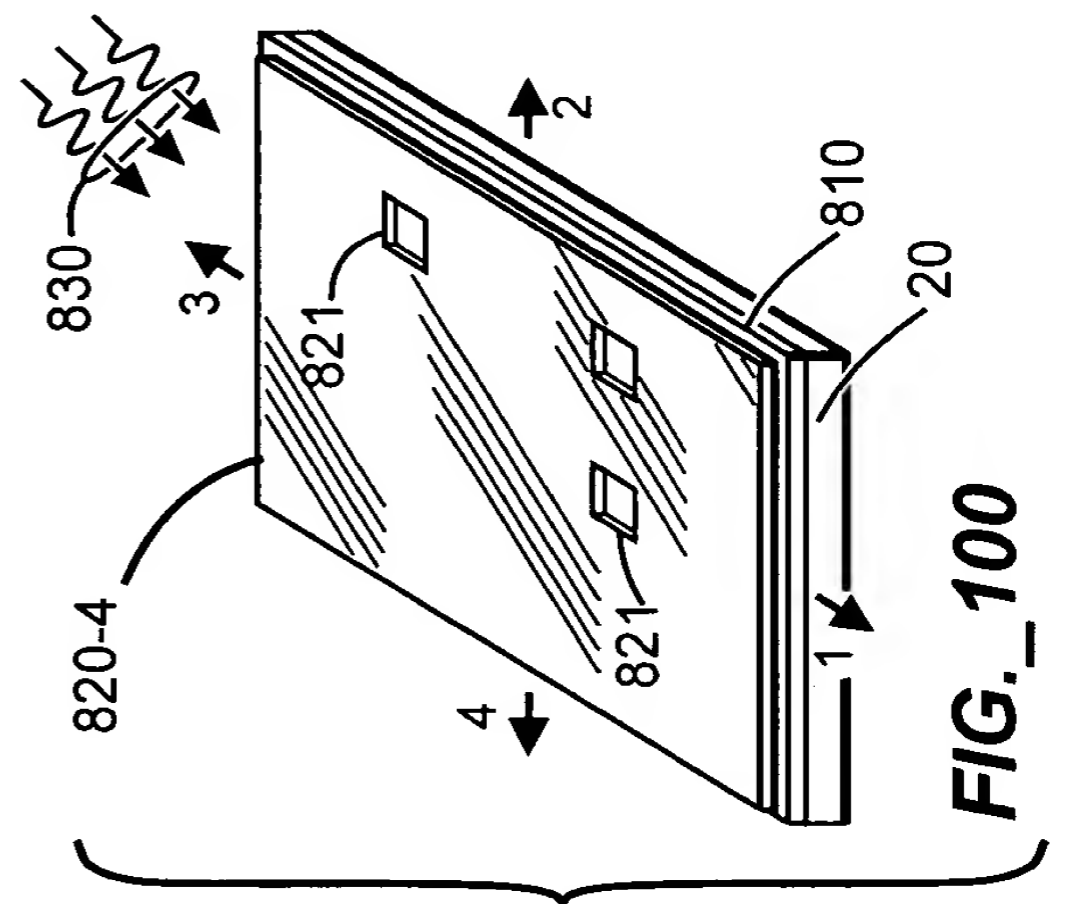
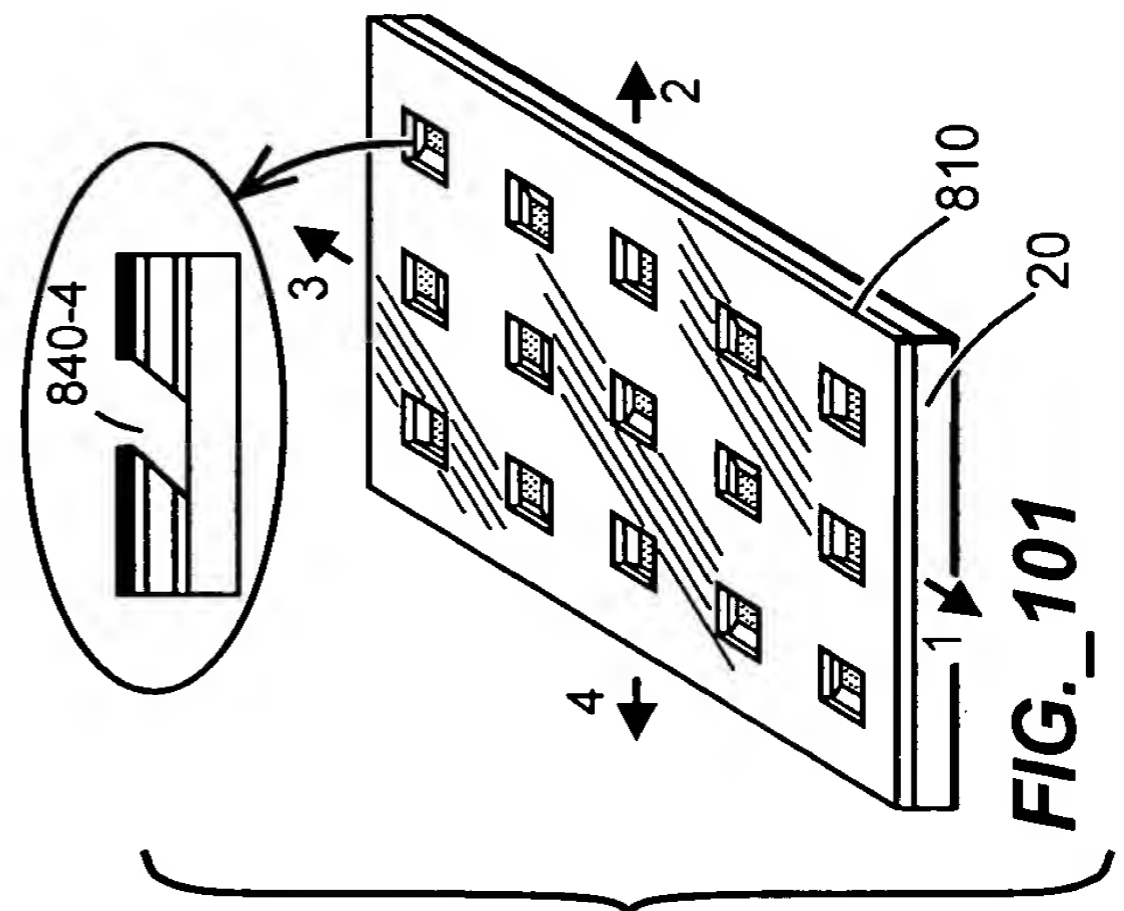
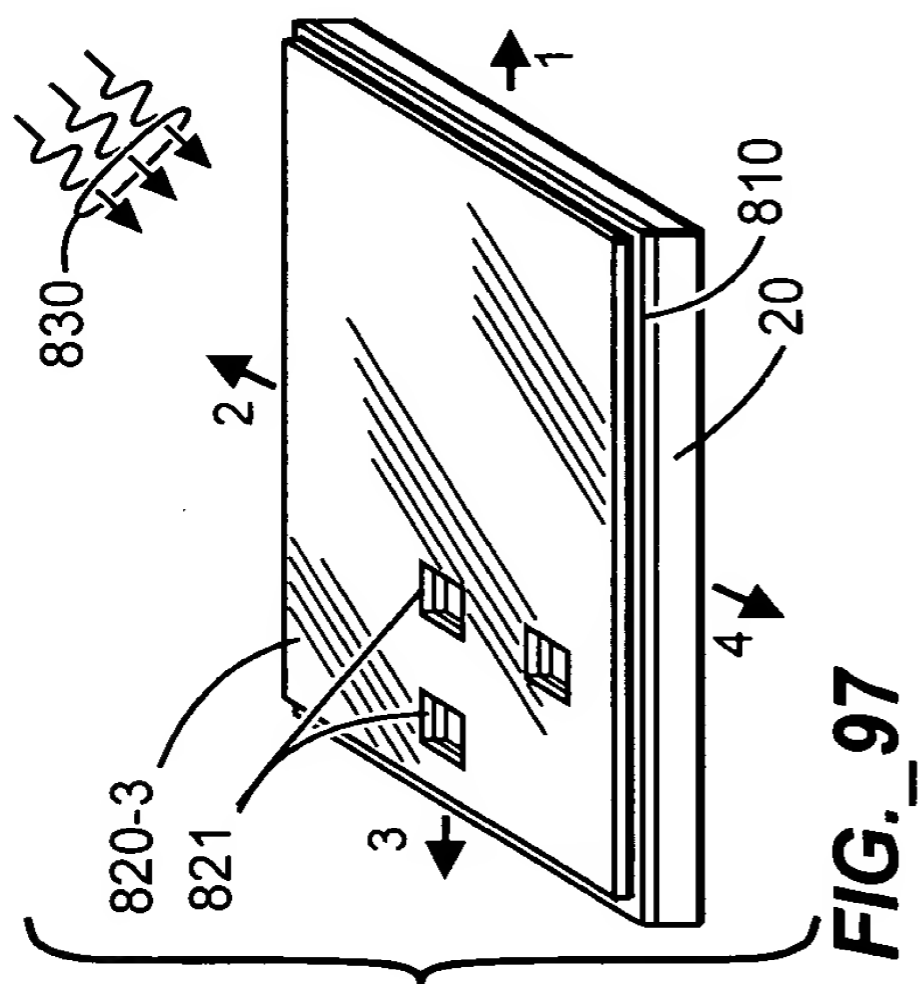
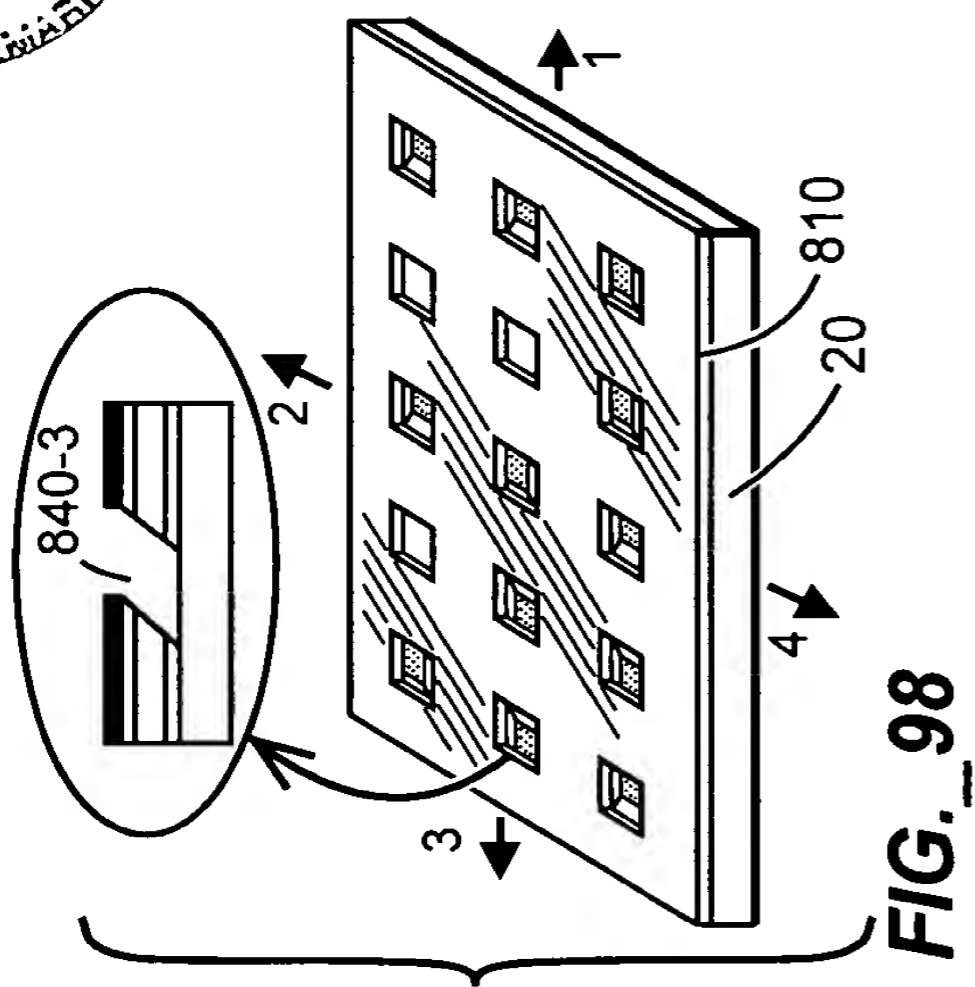
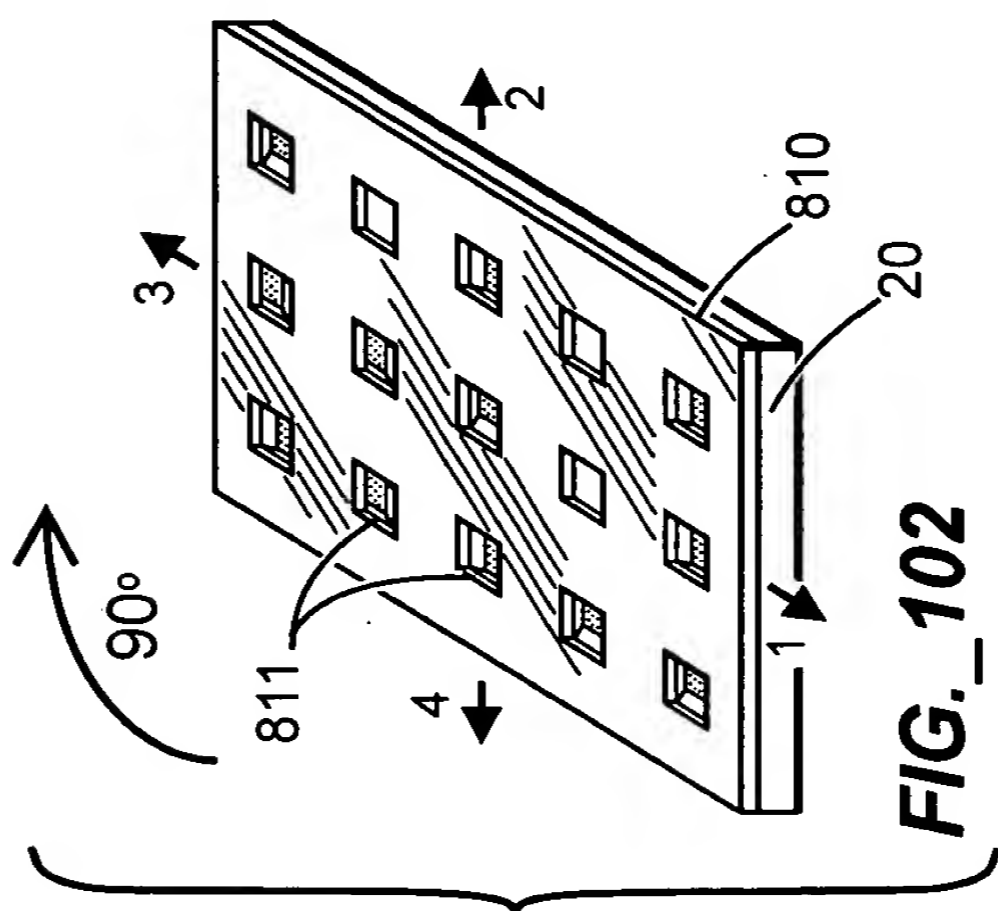
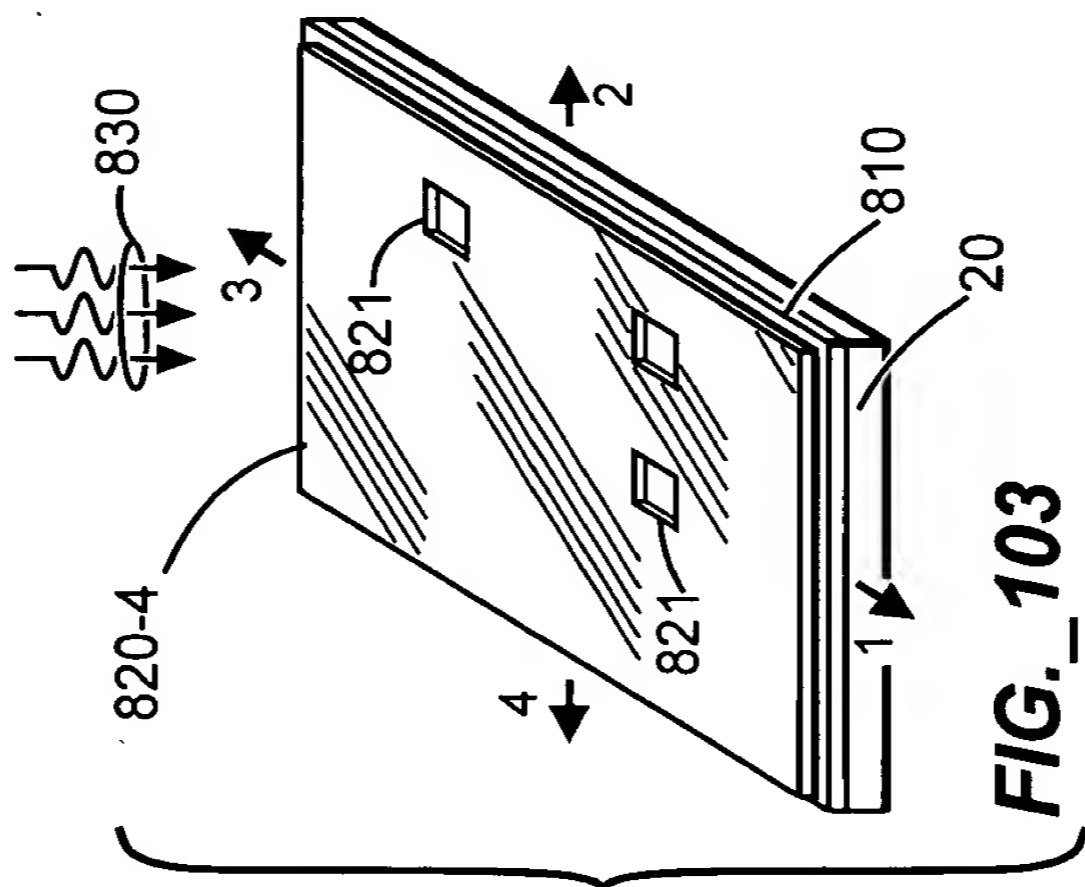
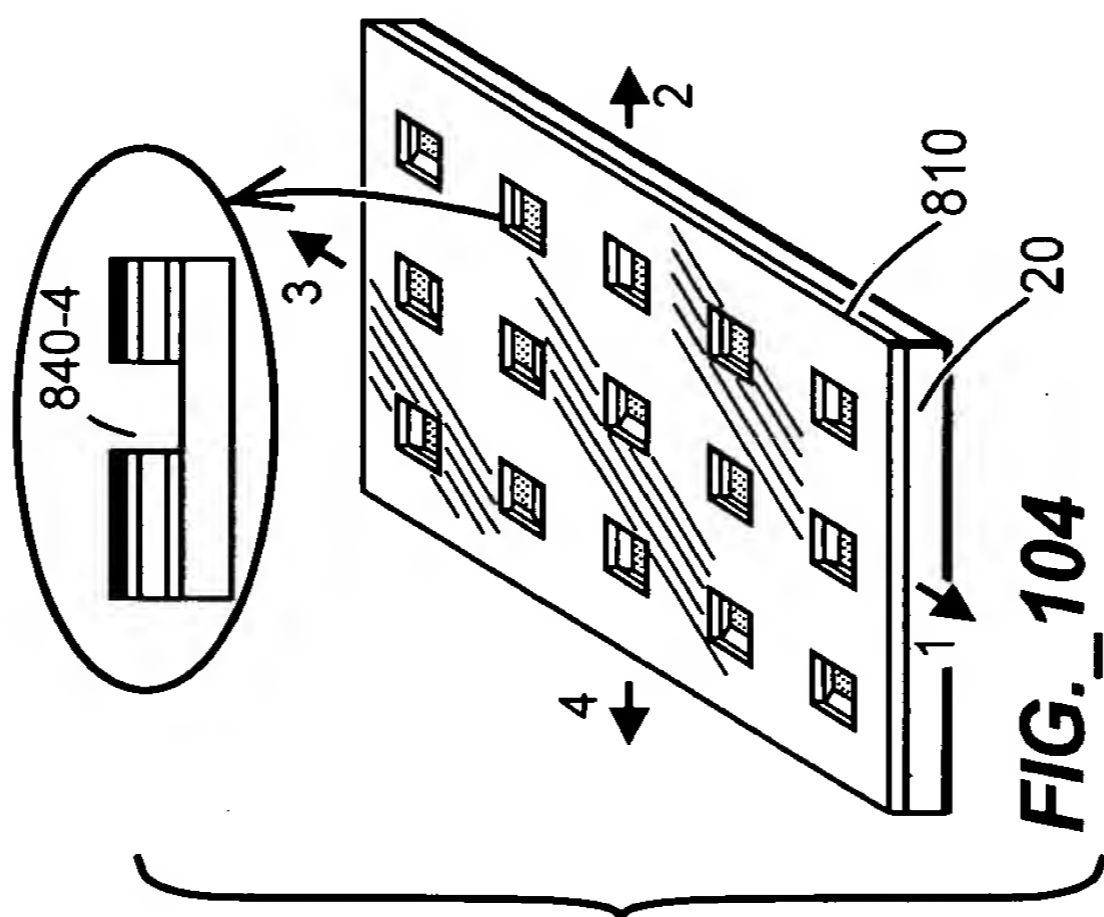


FIG._89







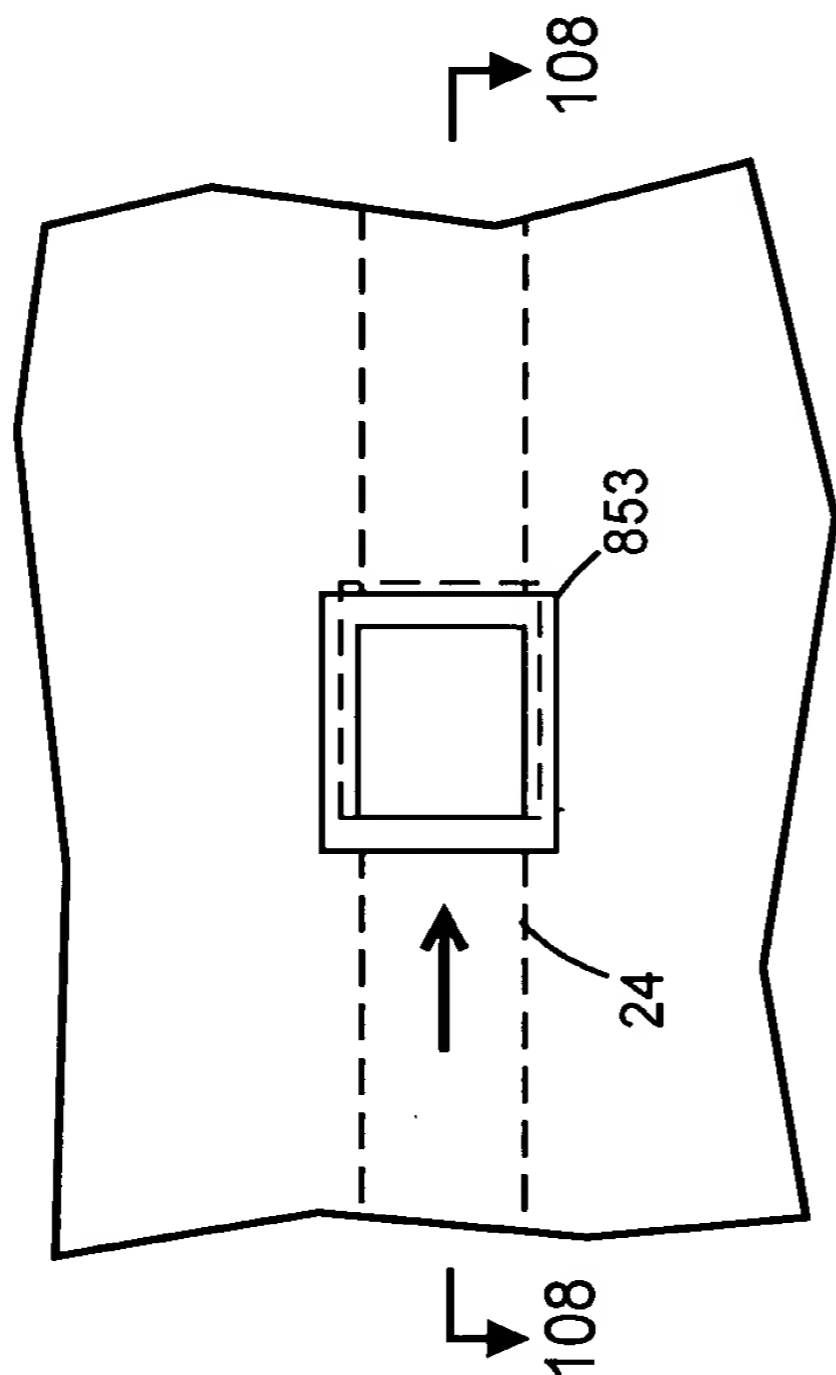


FIG. 107

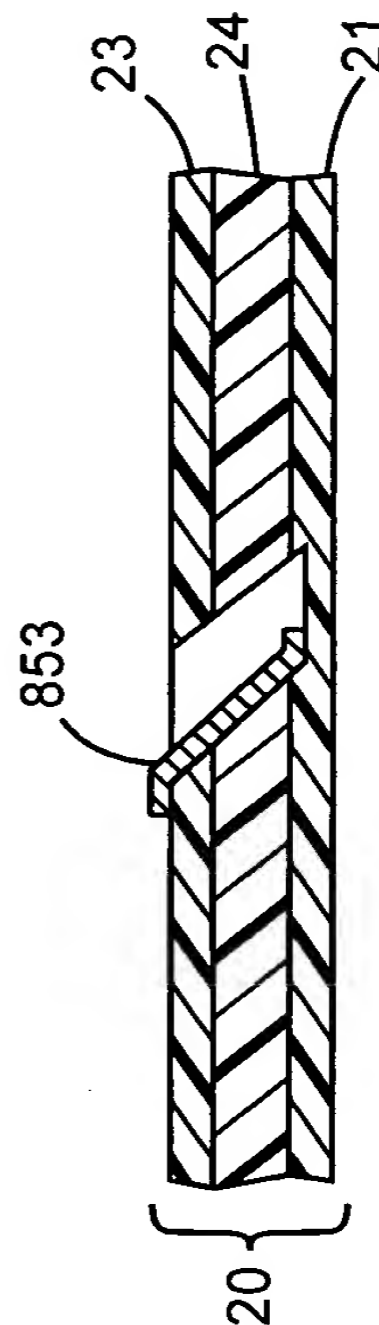


FIG. 108

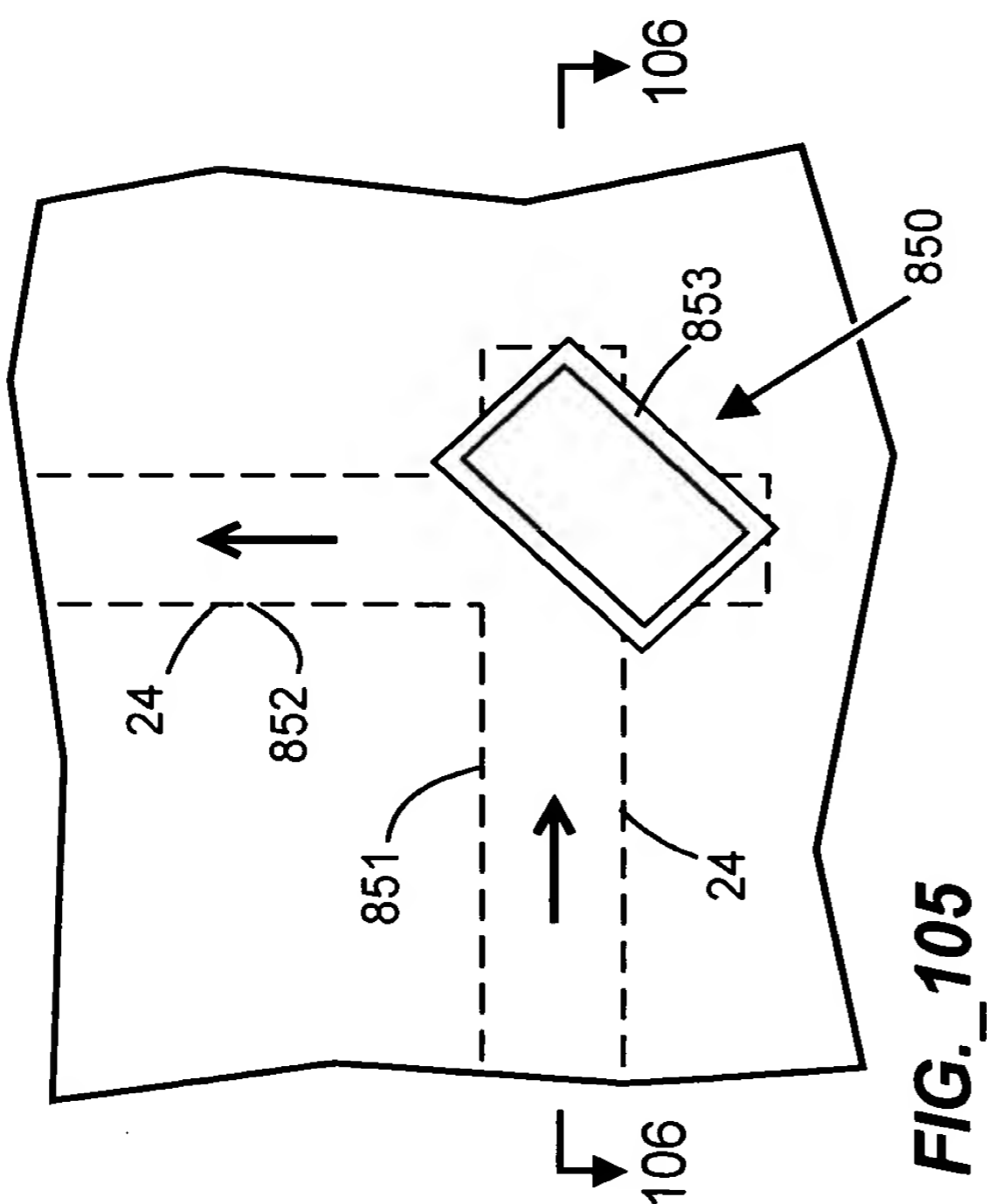


FIG. 105

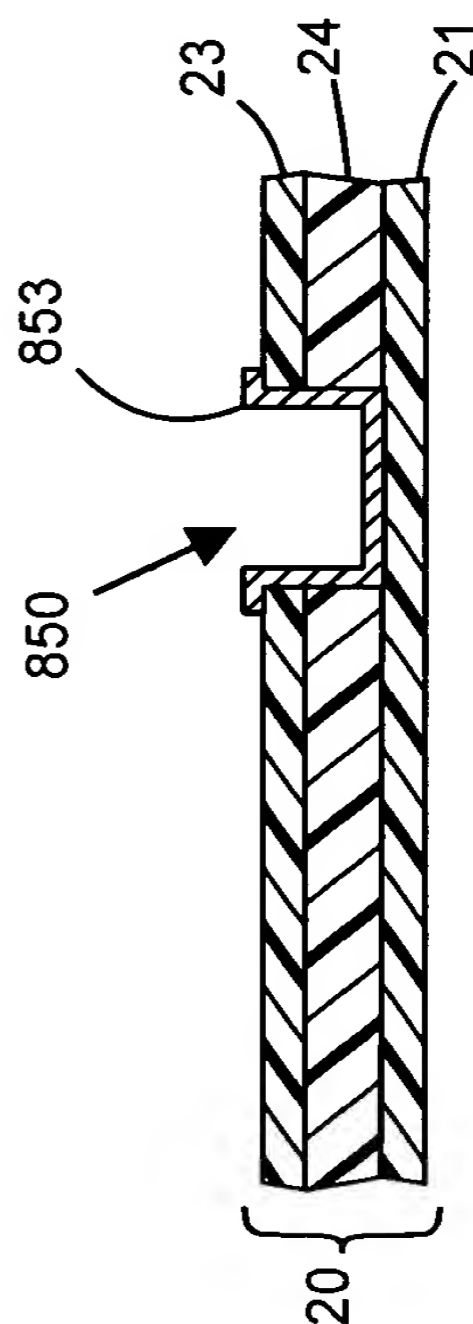


FIG. 106

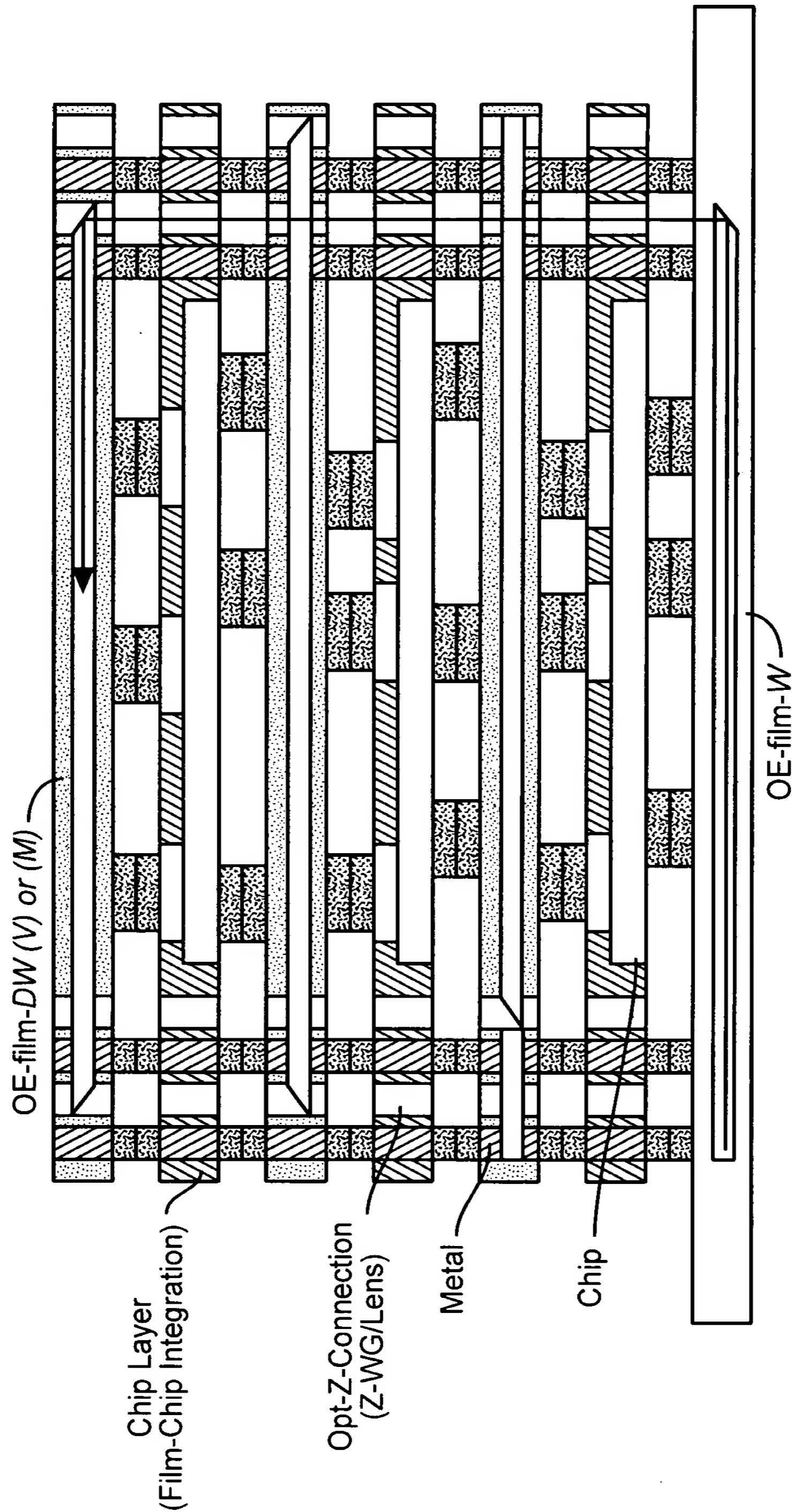


FIG. 109

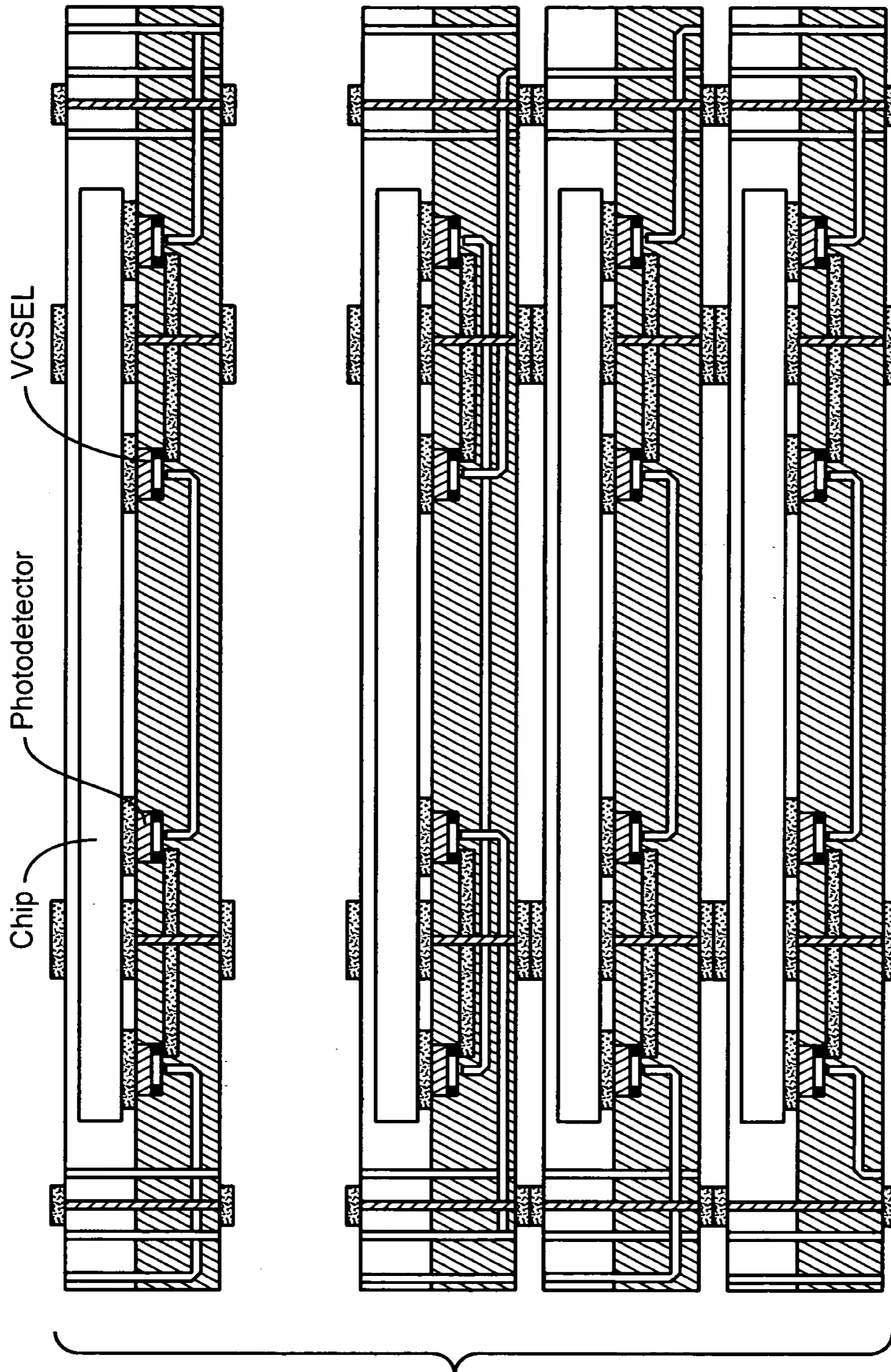


FIG._110

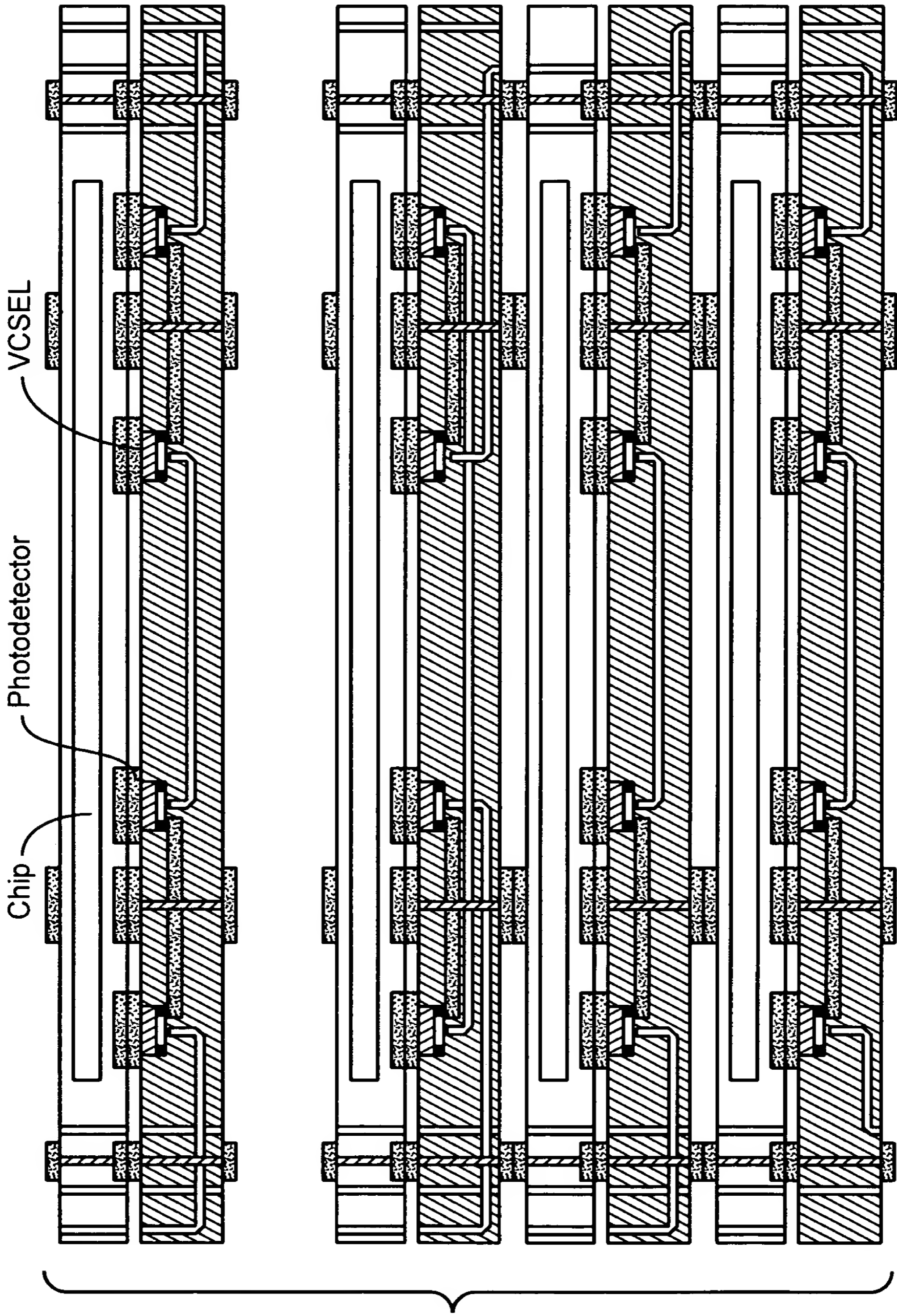
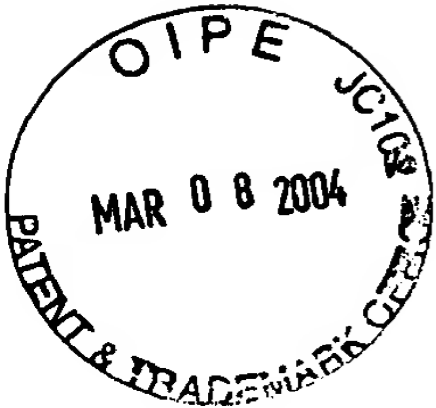


FIG. 111

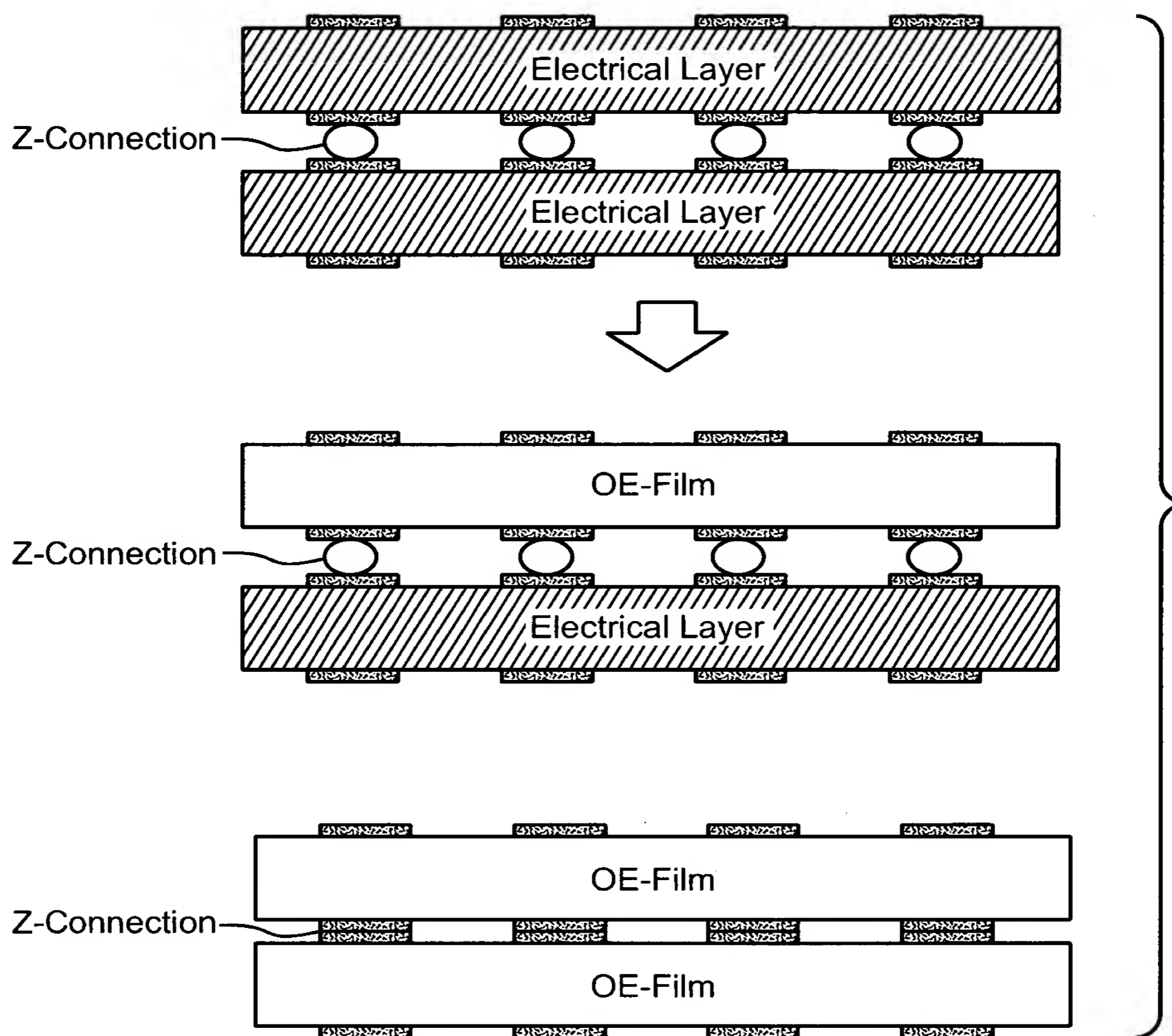
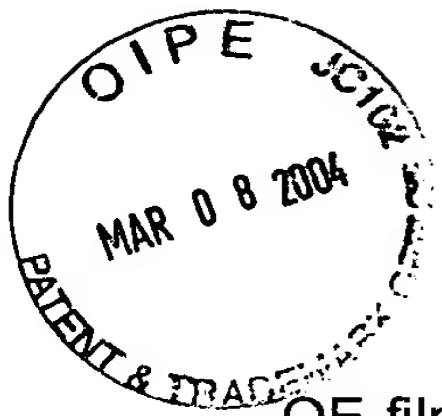


FIG._112



43 / 61

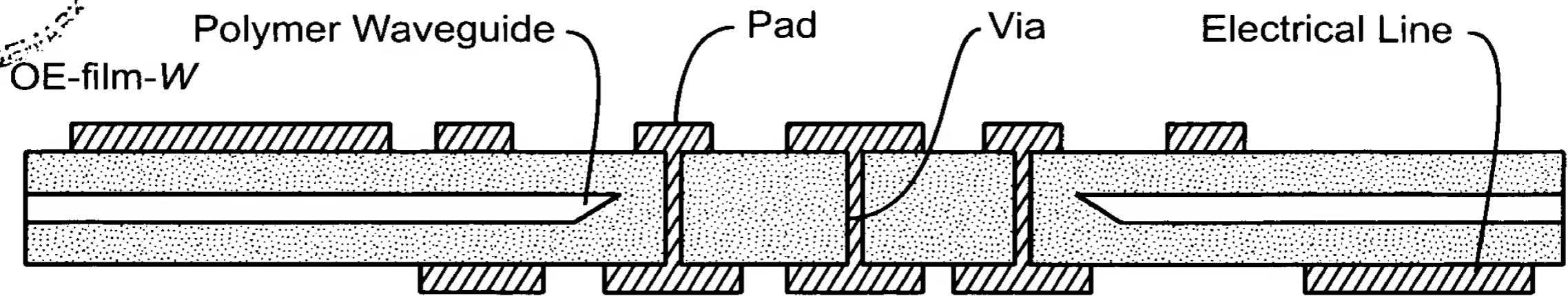


FIG. 113

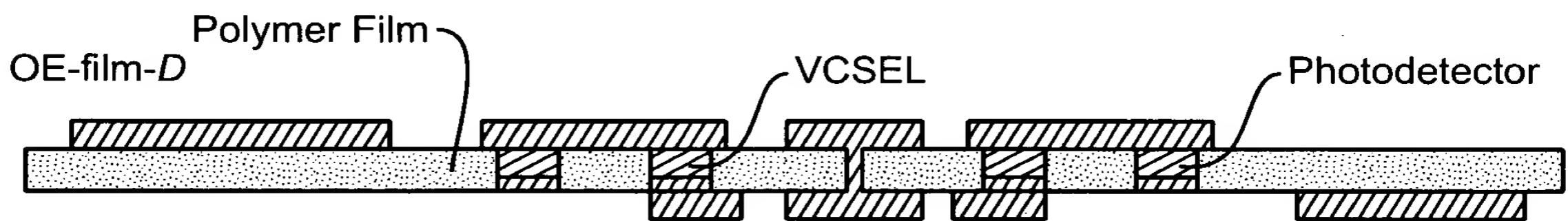


FIG. 114

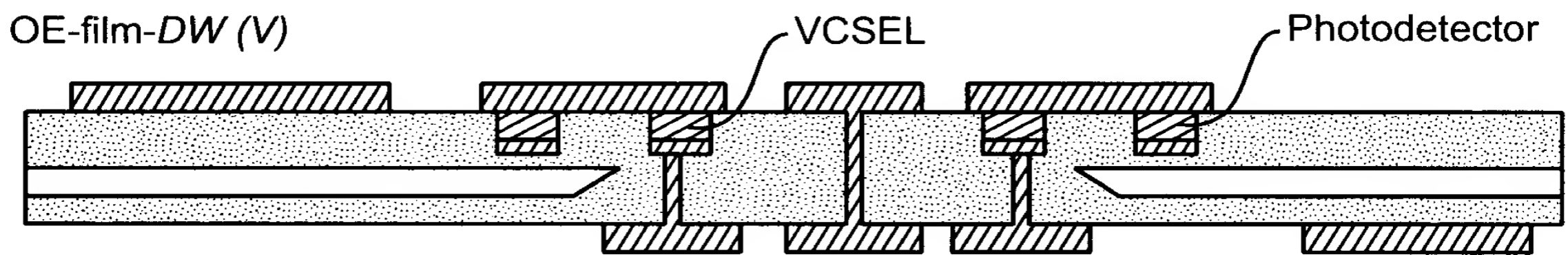


FIG. 115

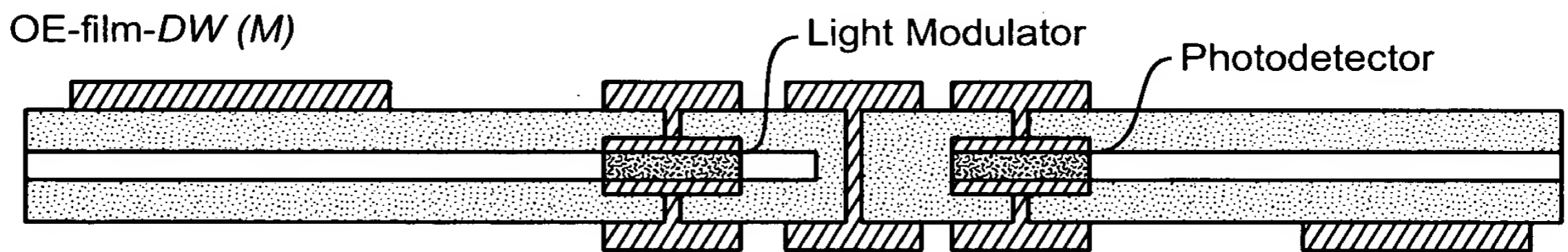


FIG. 116

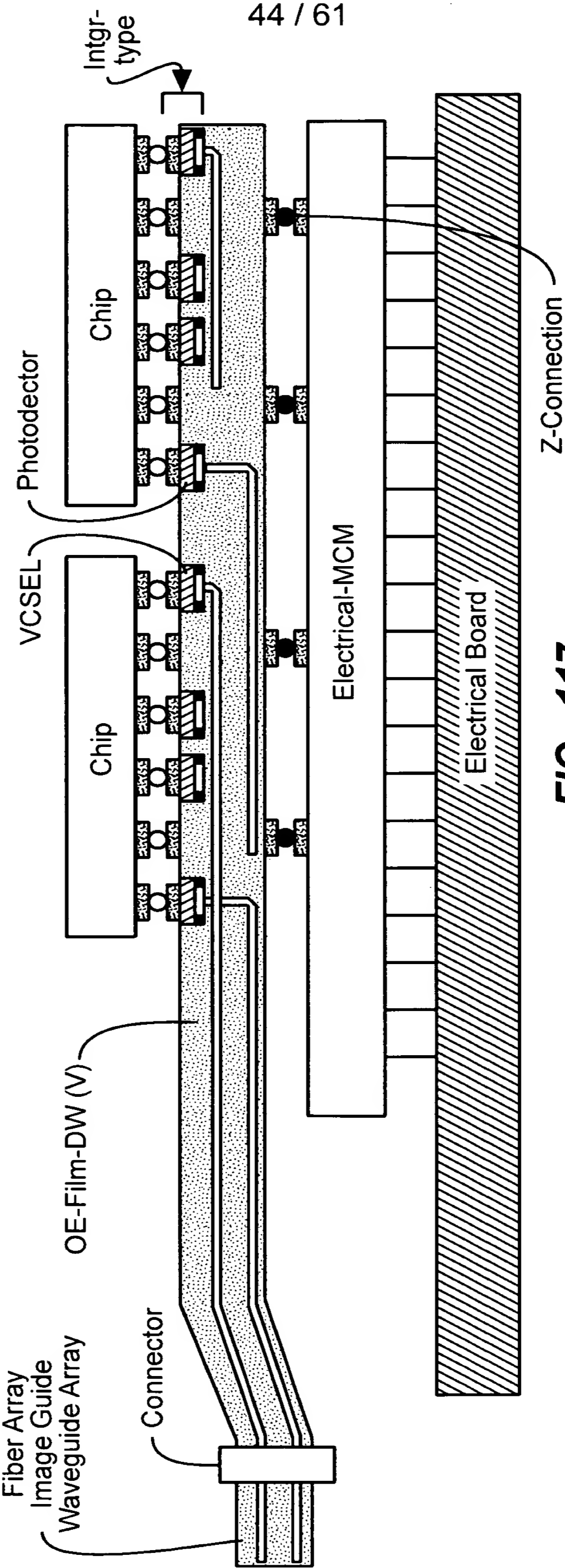


FIG._117



“Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making”

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

45 / 61

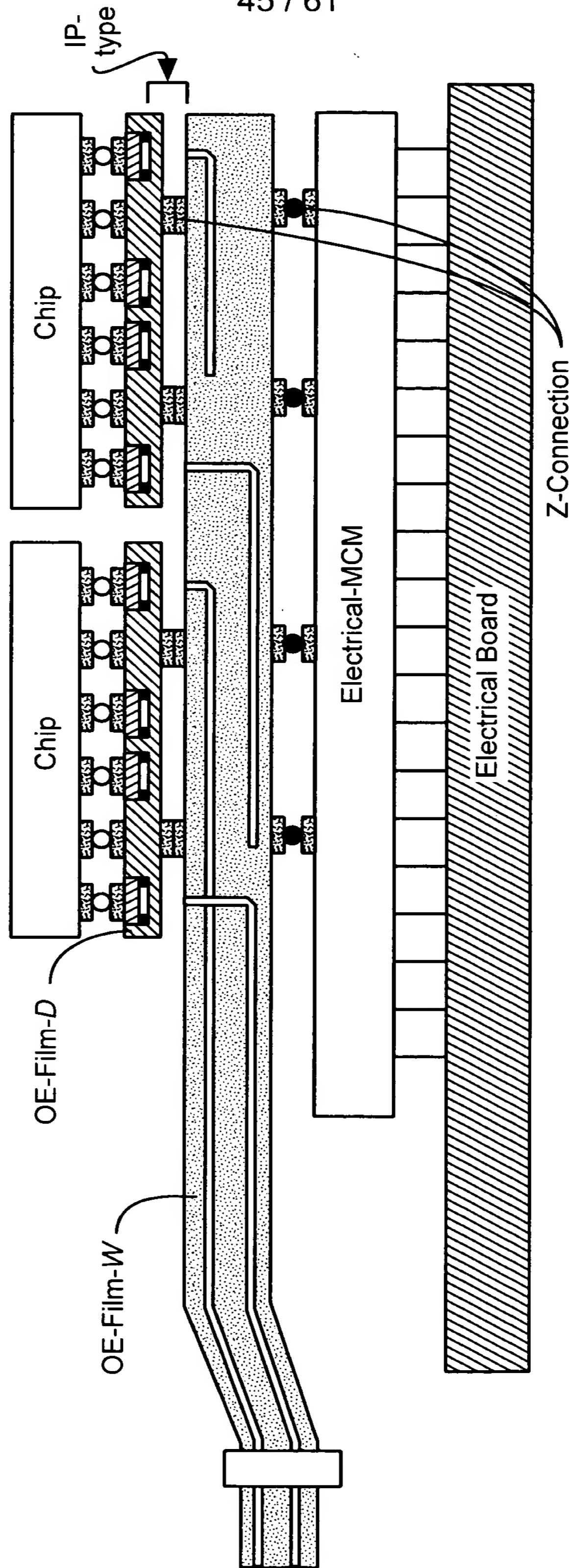


FIG._118

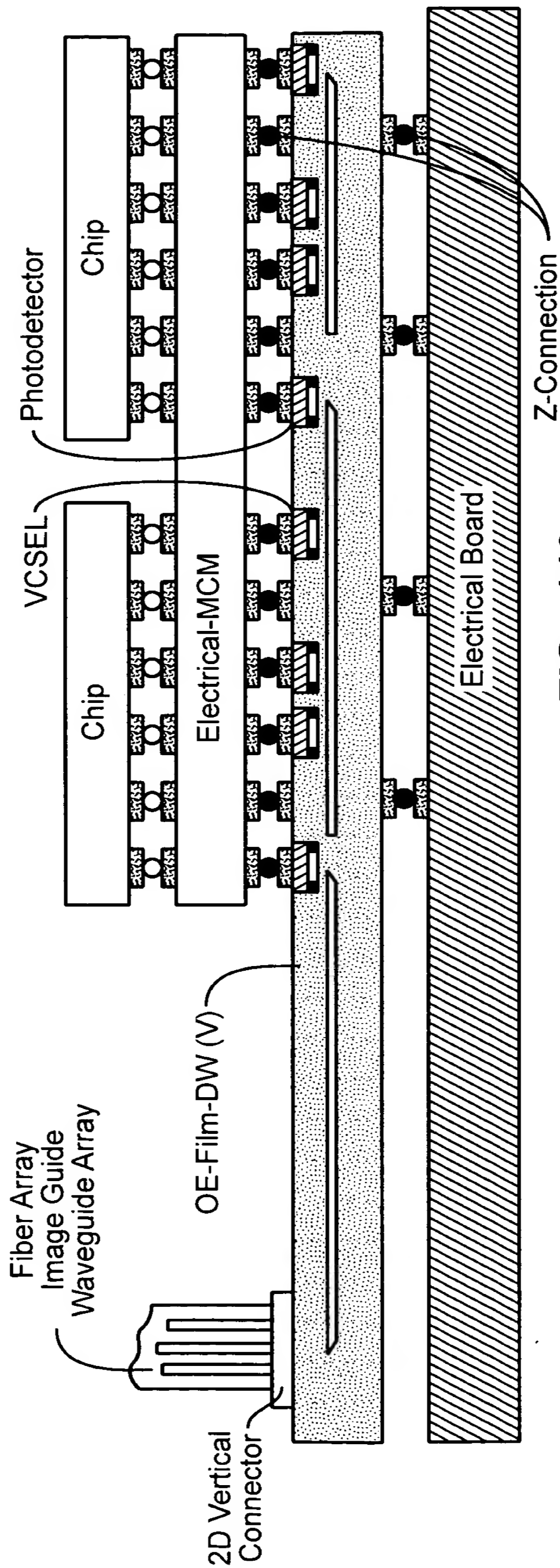


FIG. 119

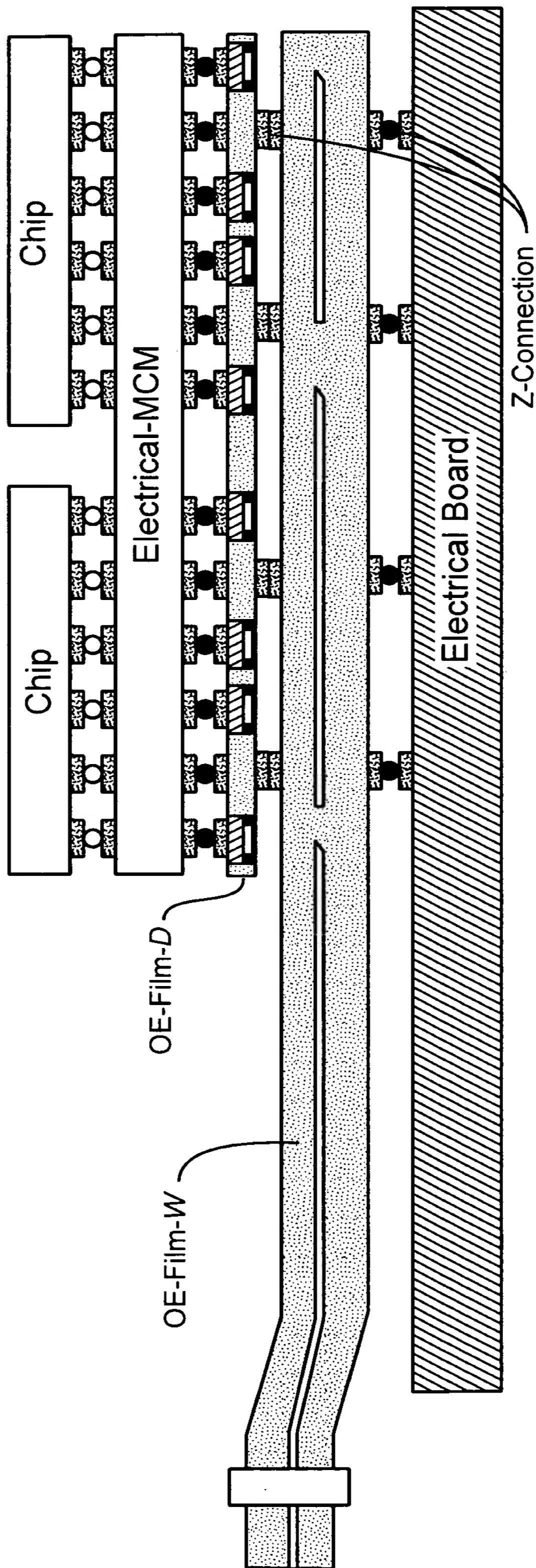


FIG._120

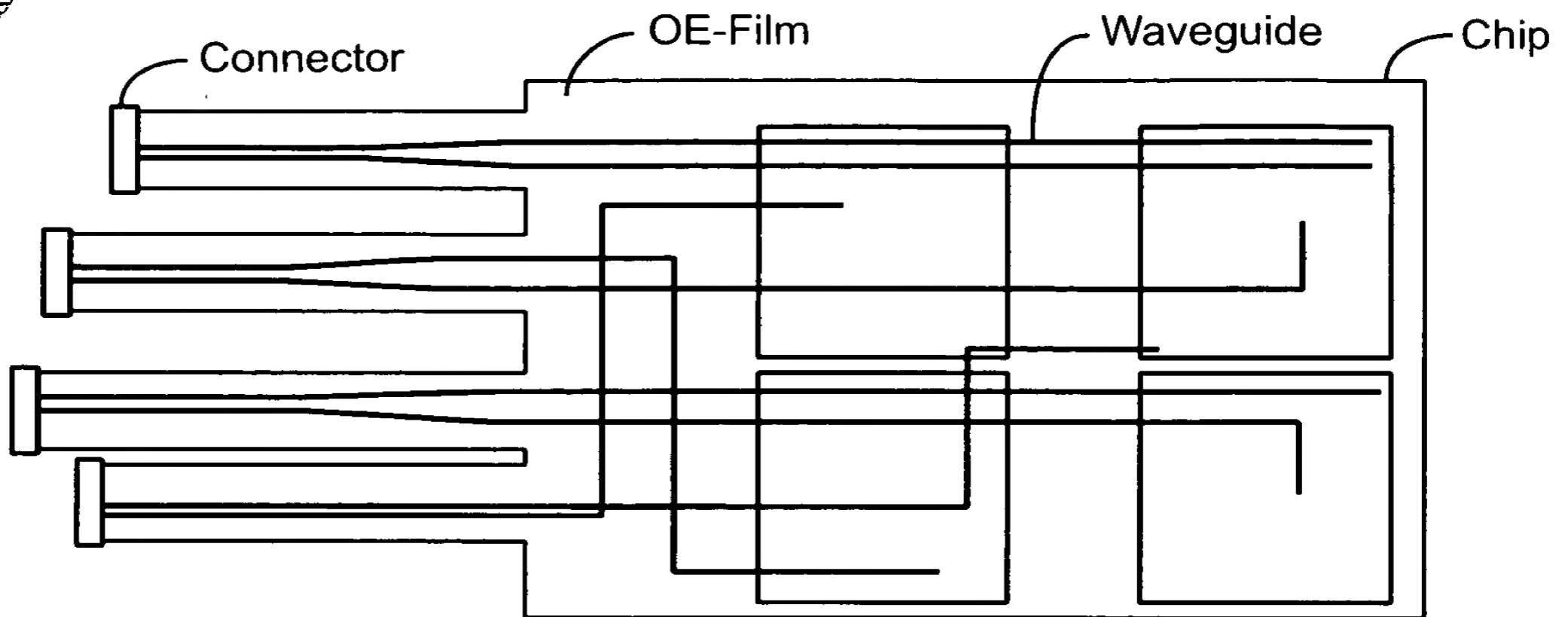
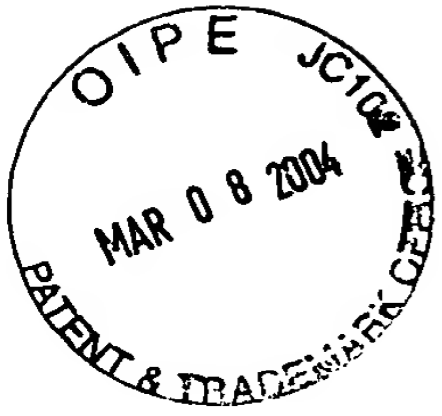


FIG. 121

Curving Part

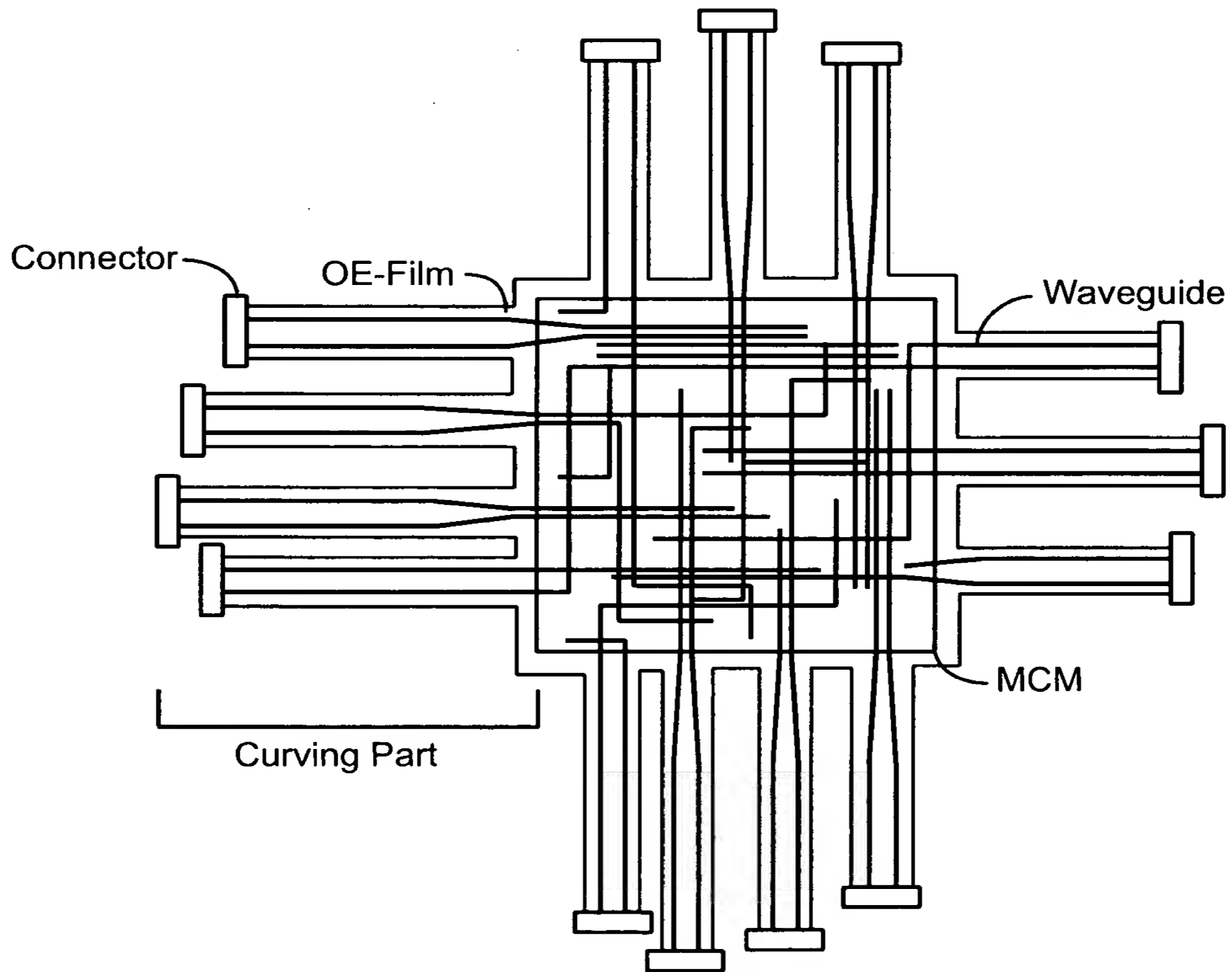


FIG. 122

Curving Part



49 / 61

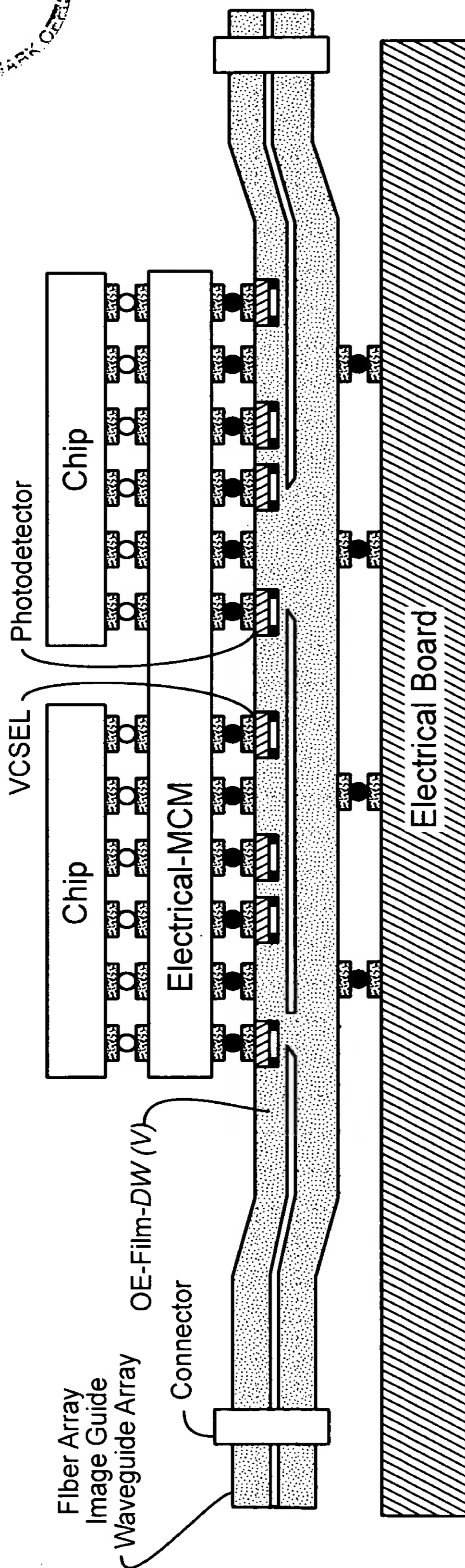


FIG. 123

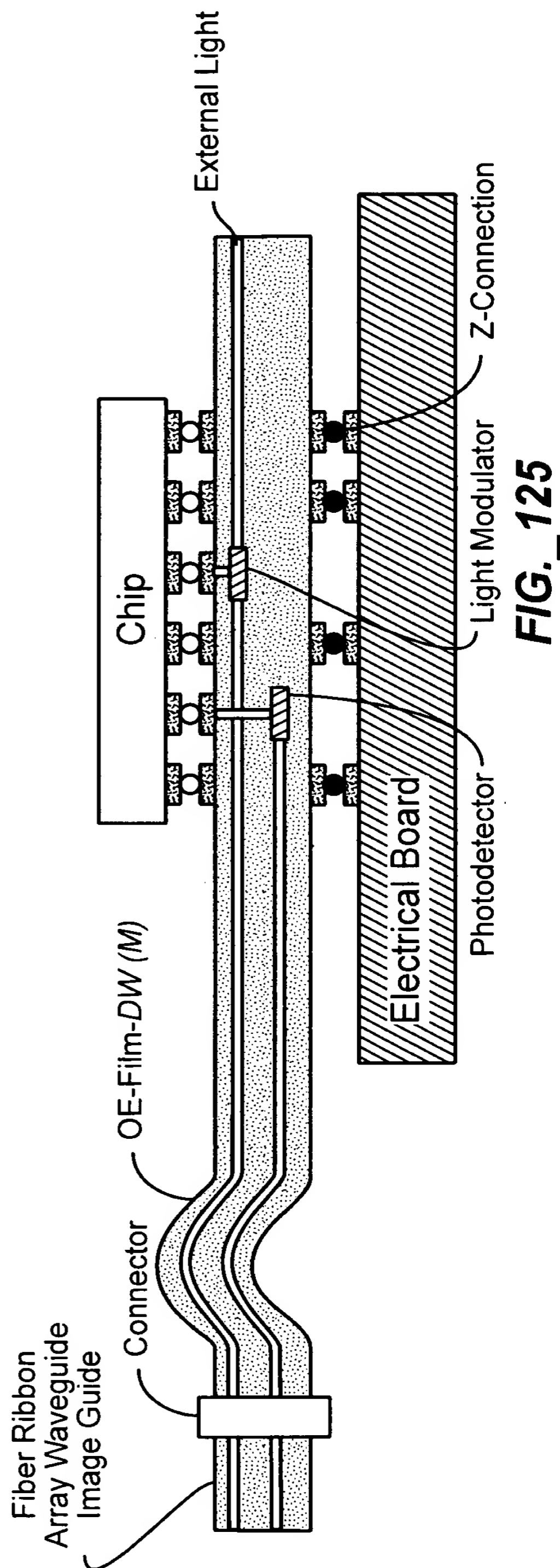


FIG. 125

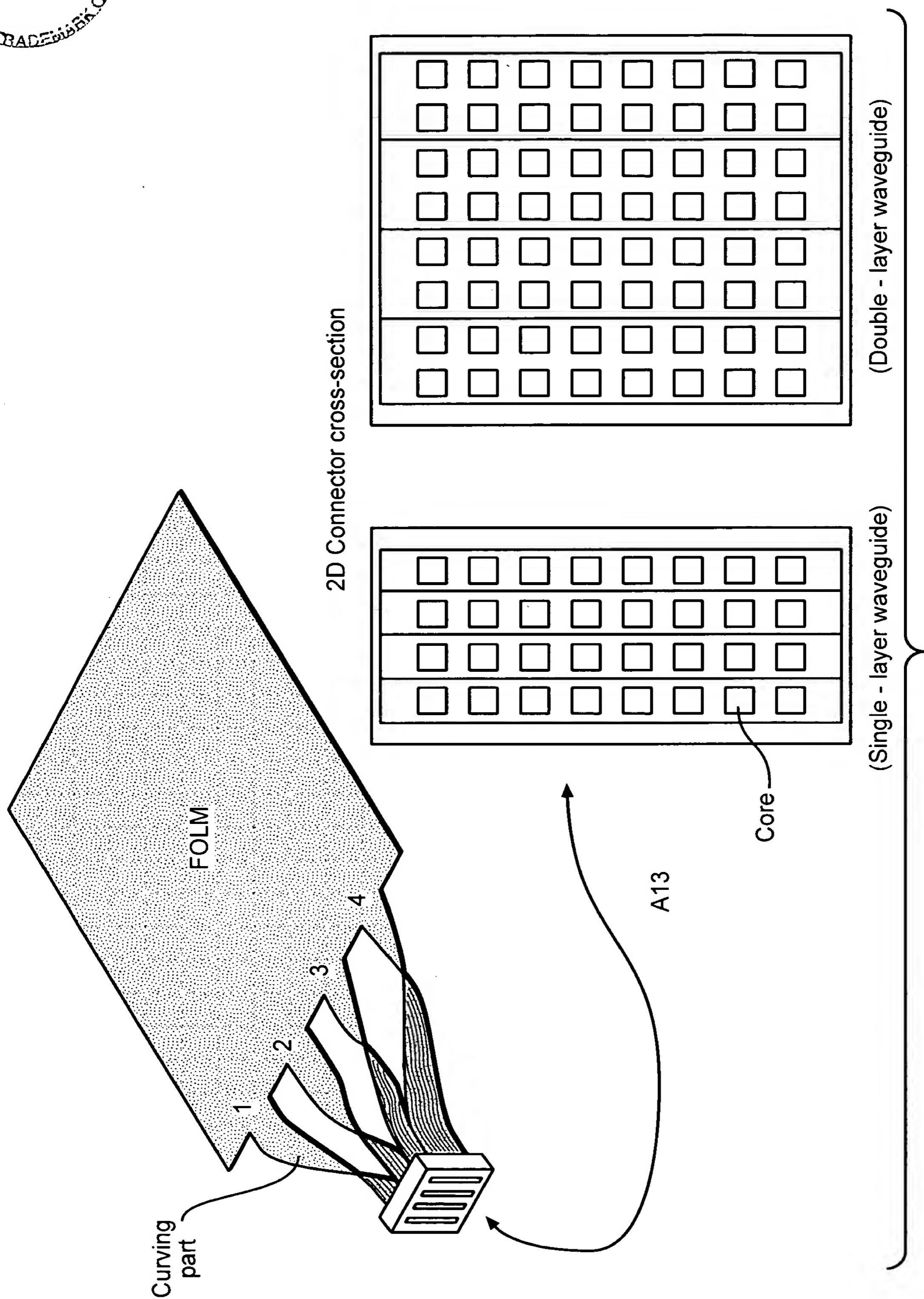


FIG. 124

Through Put: 1.5 pbs x 196 ch Assume SSX MCM Size is 5 cm x 5 cm

FIG. 126

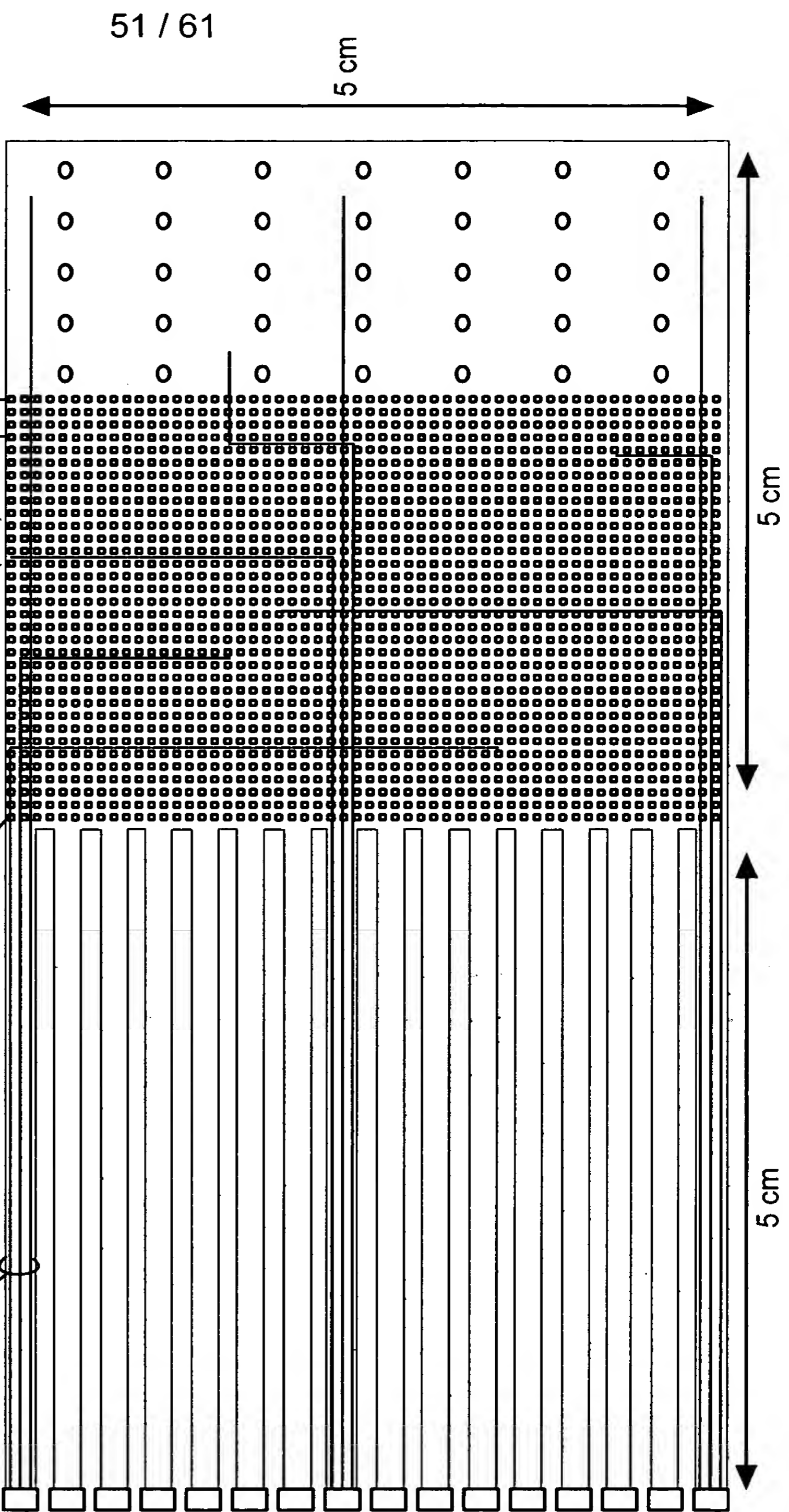
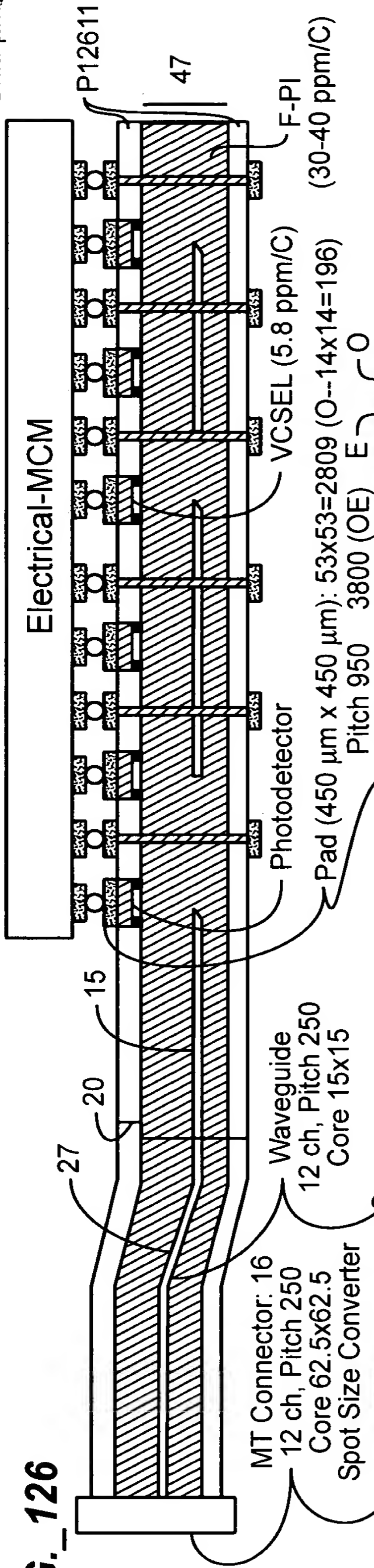


FIG. 127



FIG._129

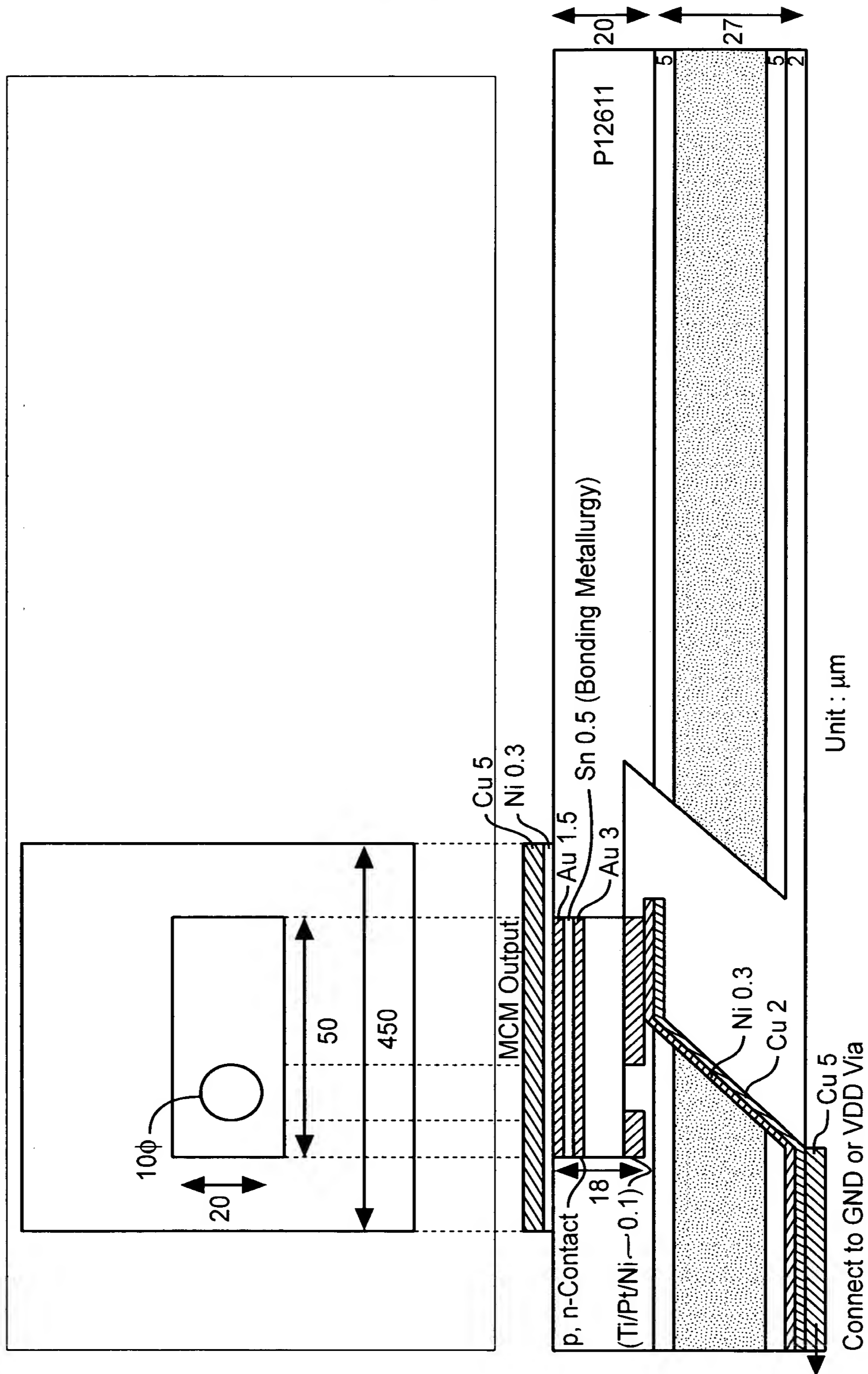


FIG._128

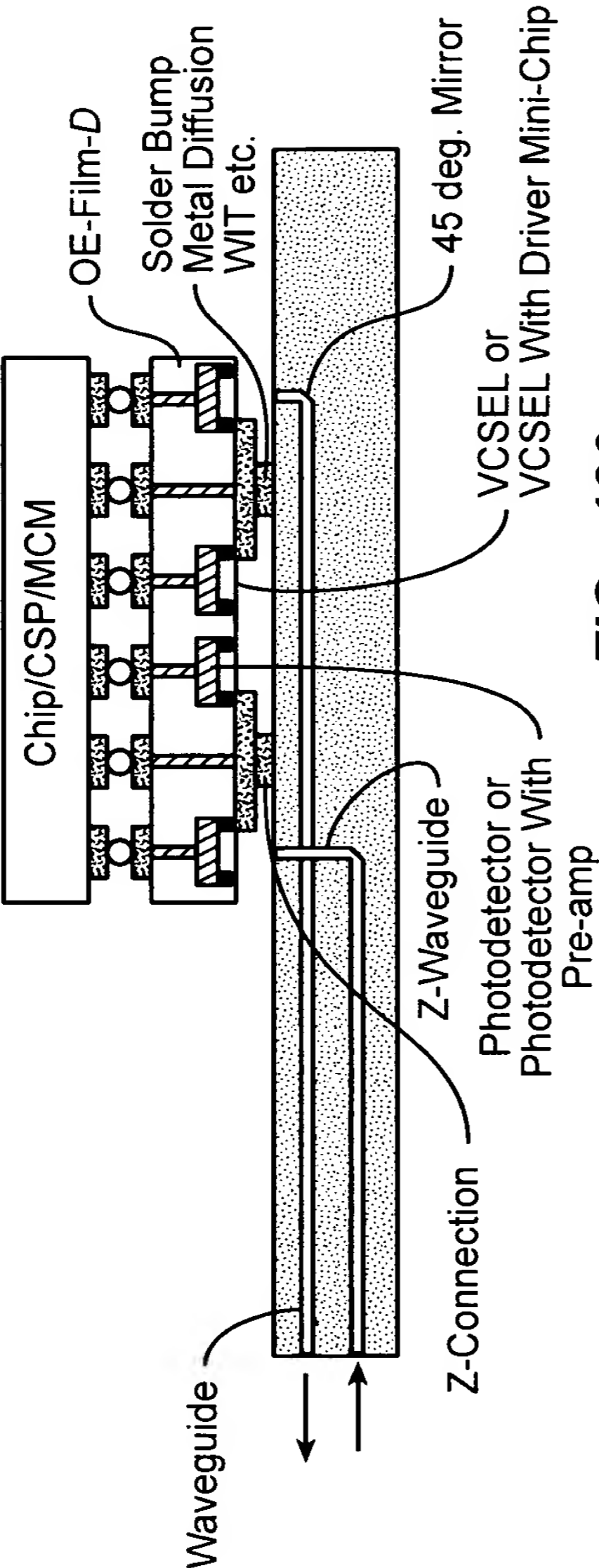


FIG. 130

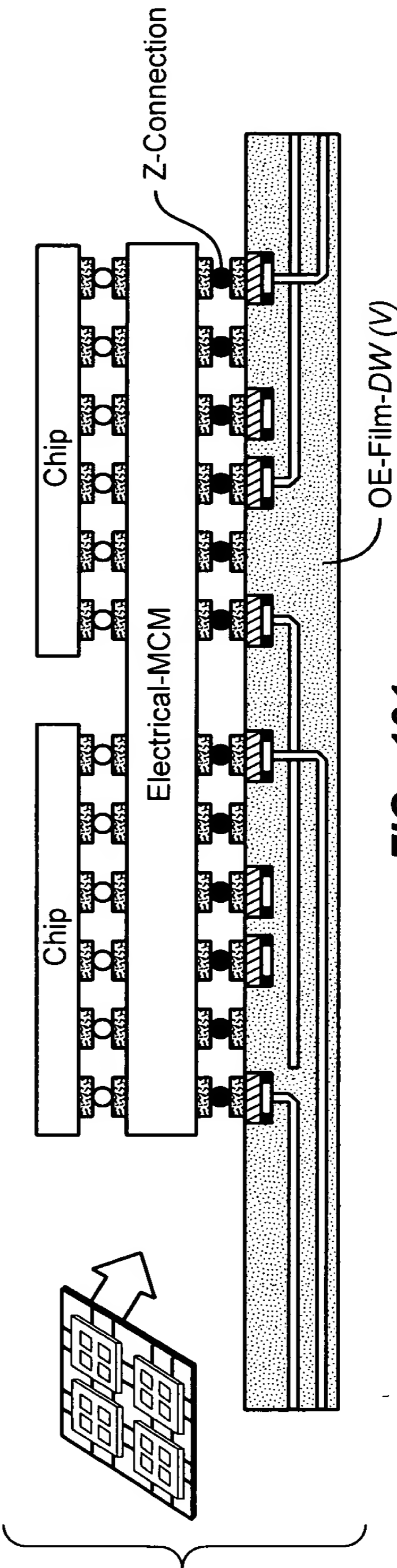


FIG. 131

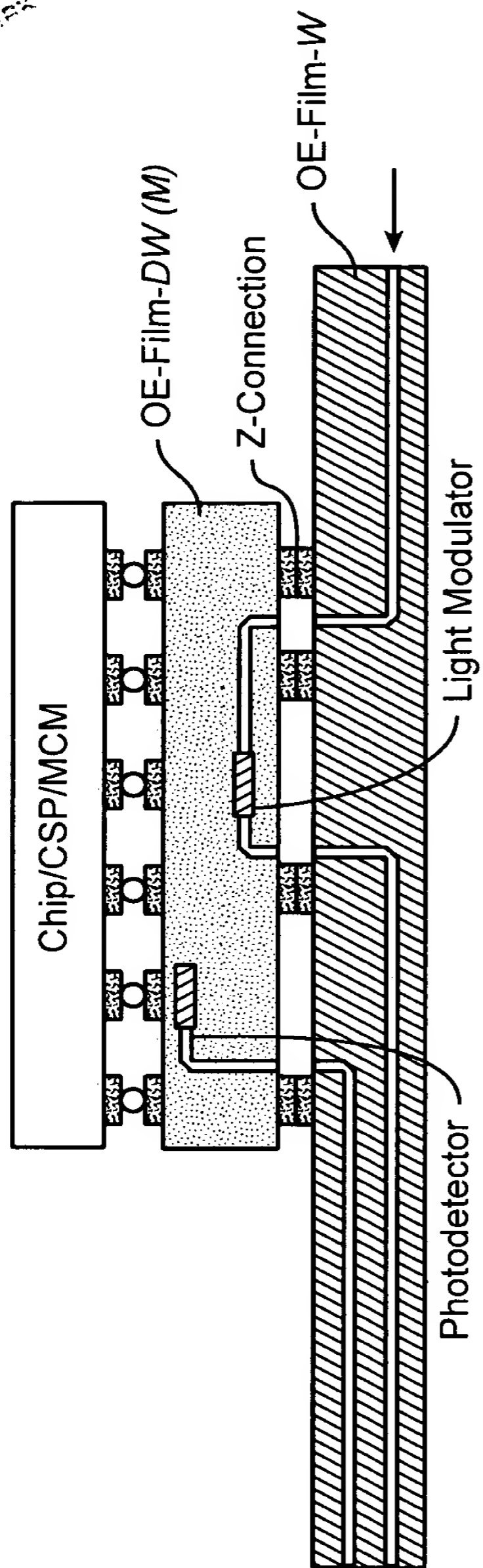


FIG._132

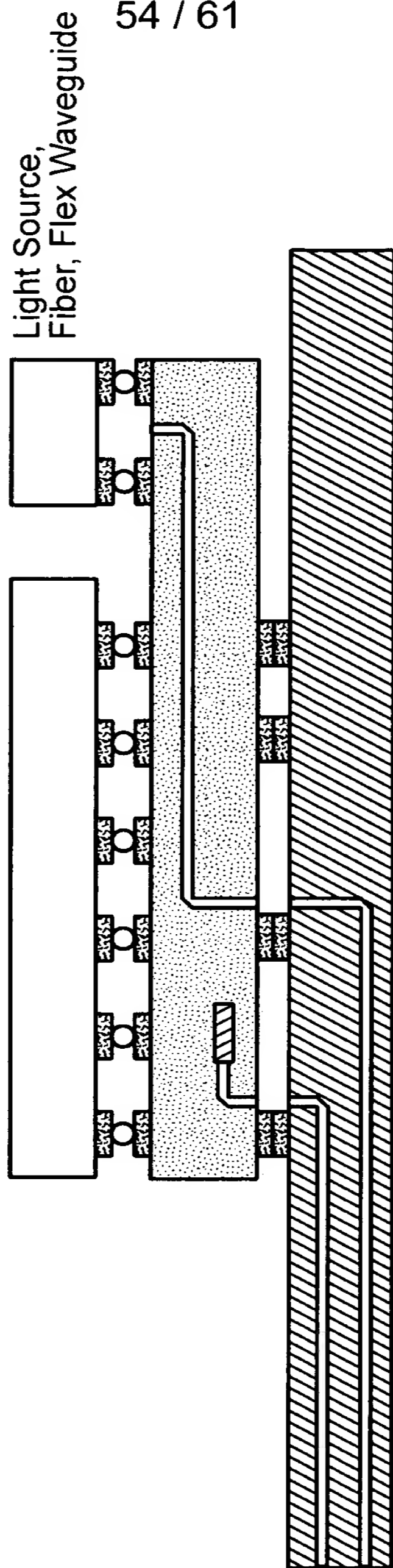


FIG._133

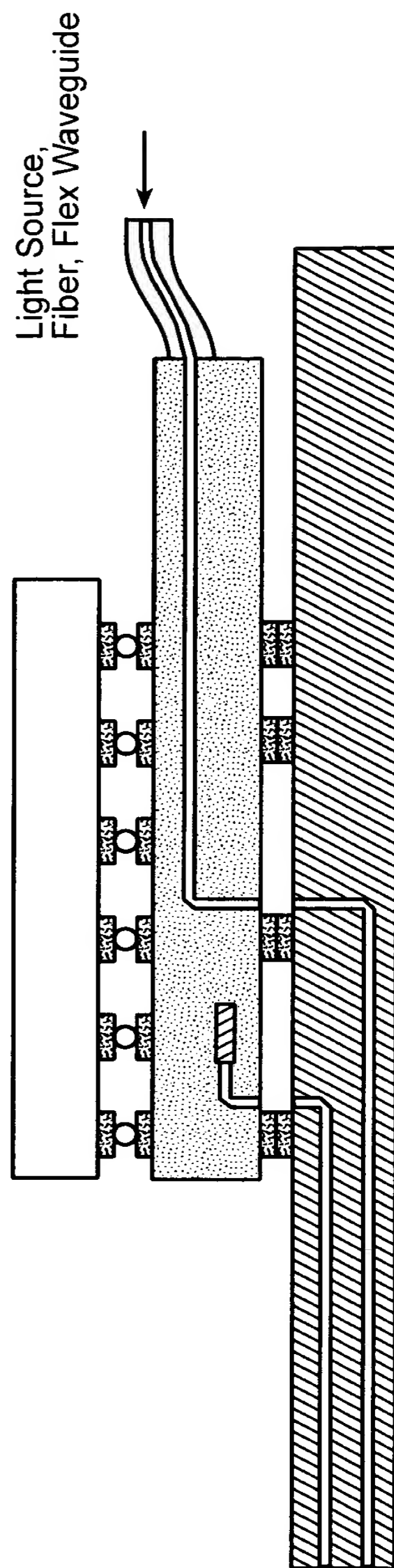


FIG._134



“Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making”

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

55 / 61

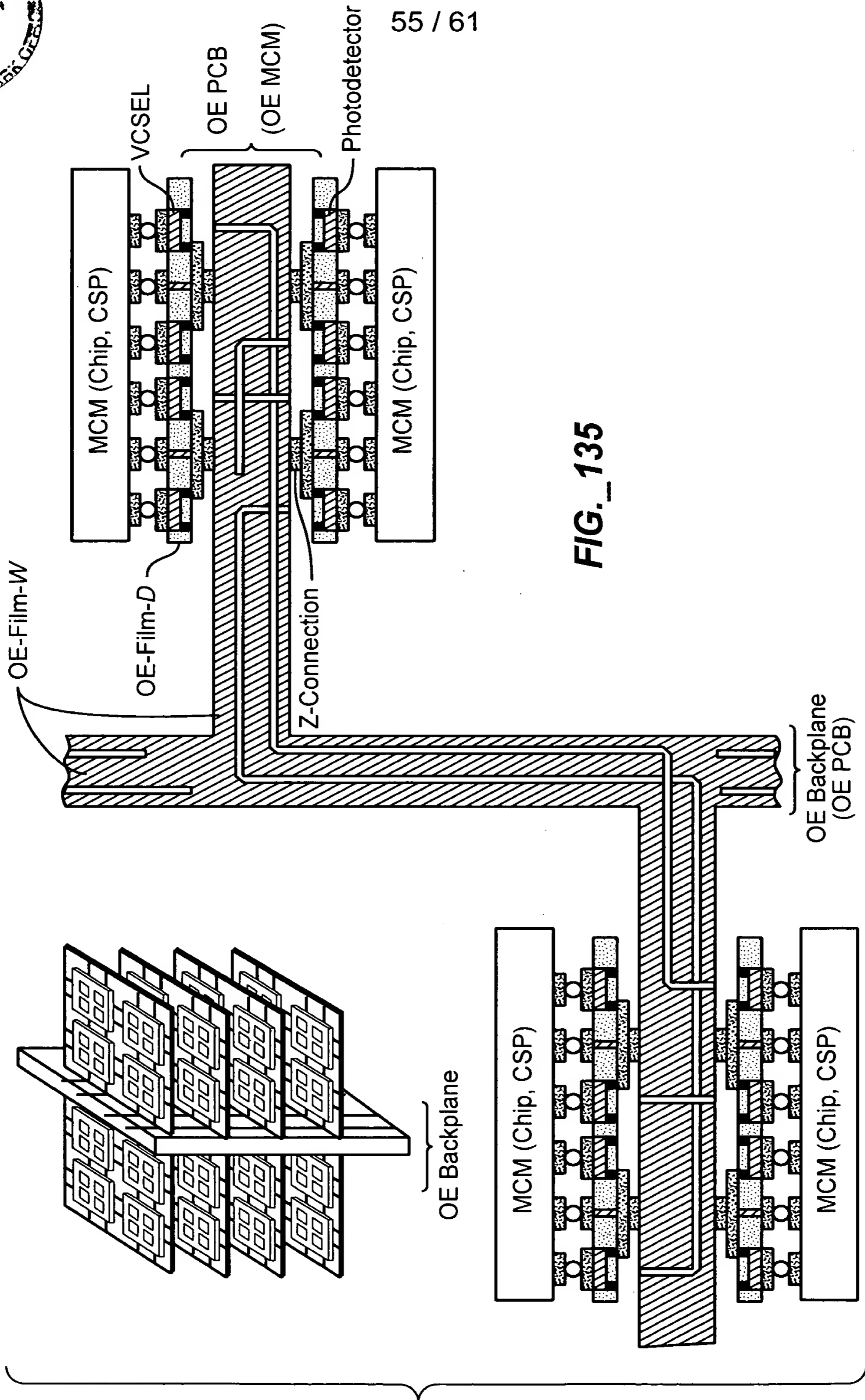


FIG. 135



"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

56 / 61

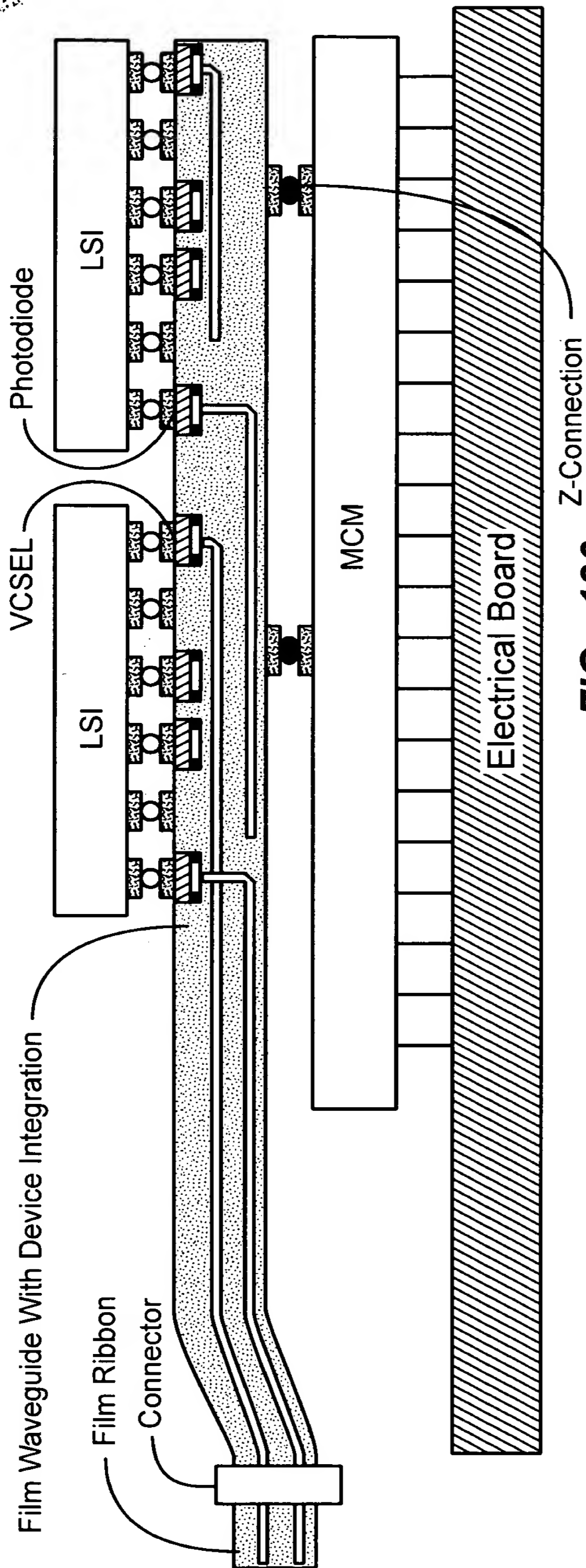


FIG. 136

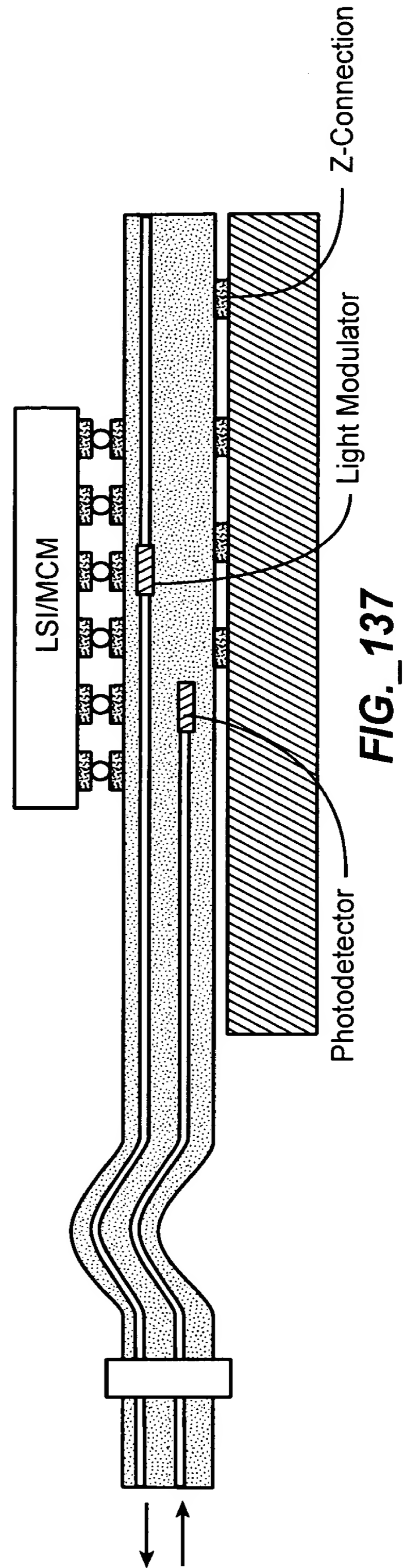
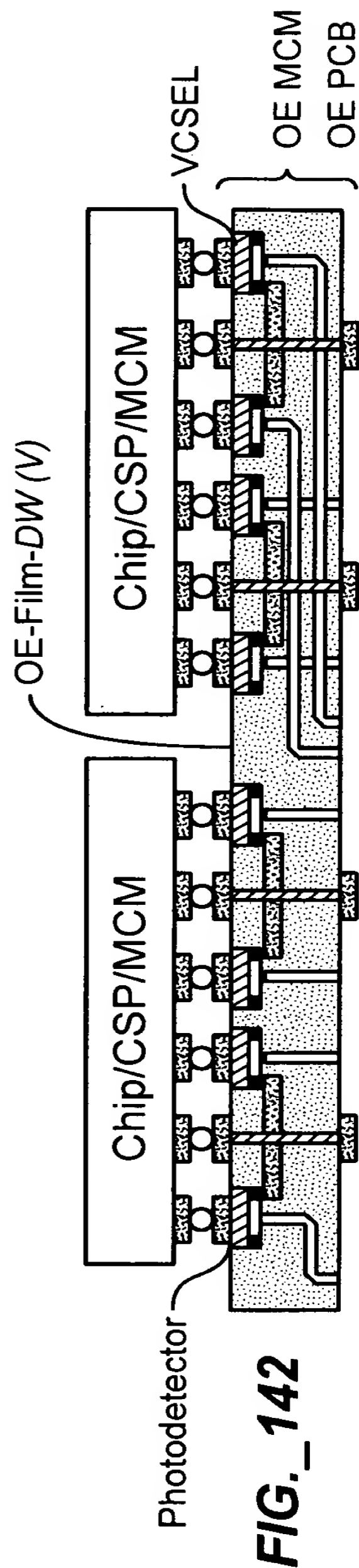
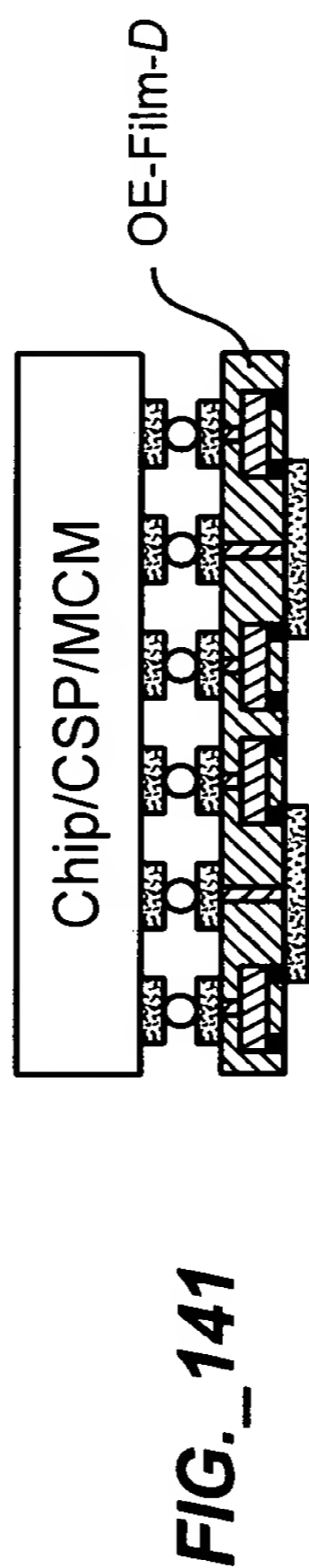
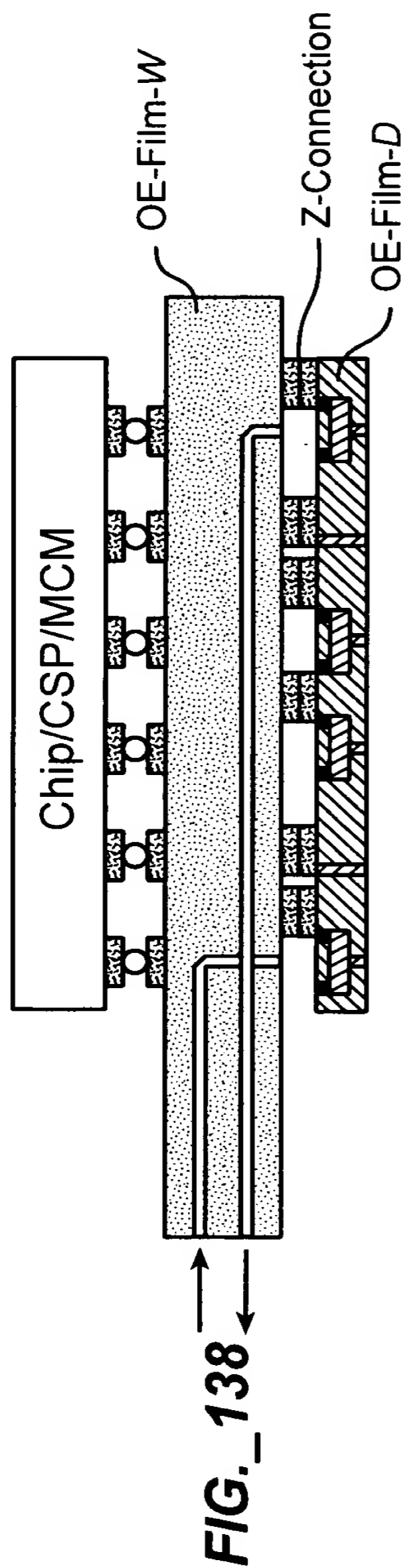


FIG. 137



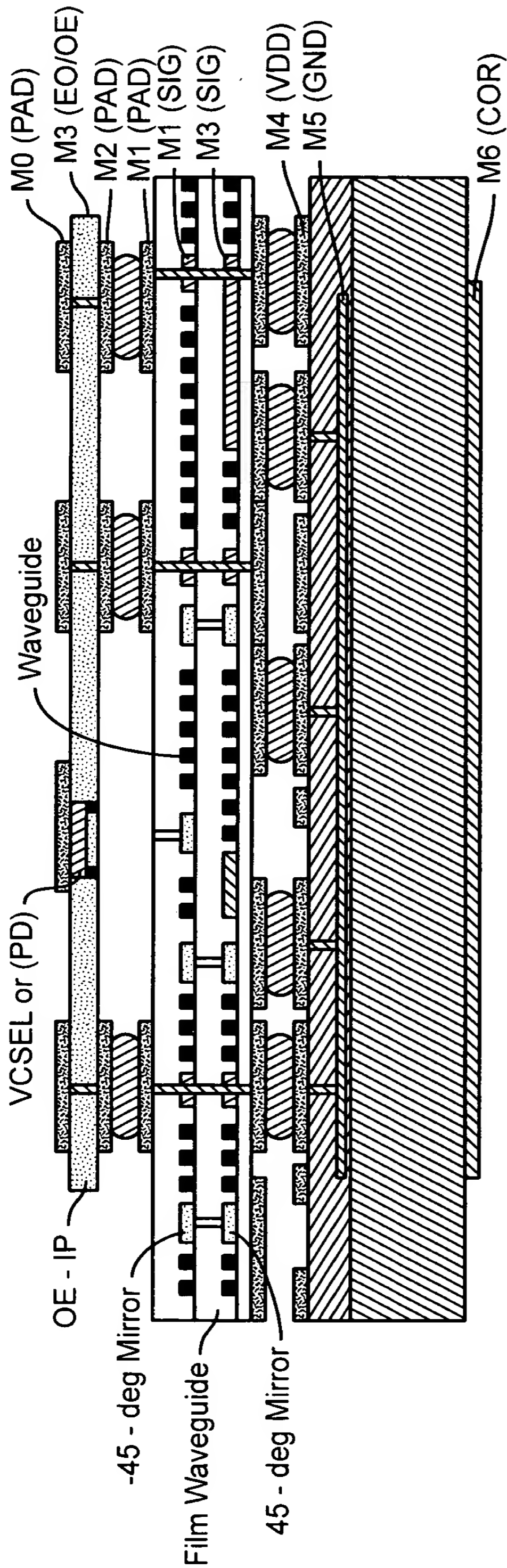


FIG. 139

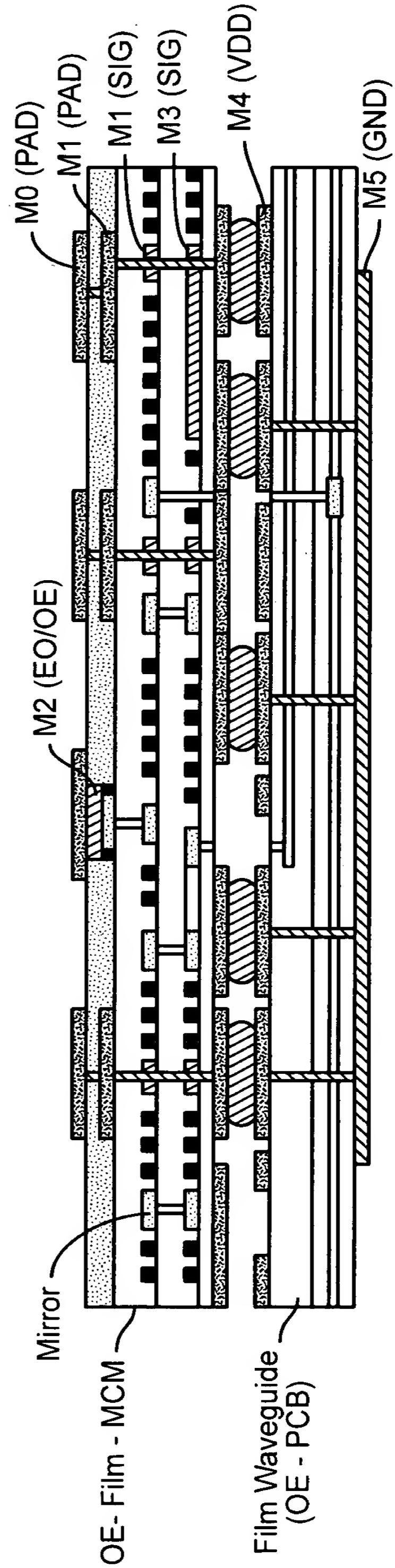


FIG. 140

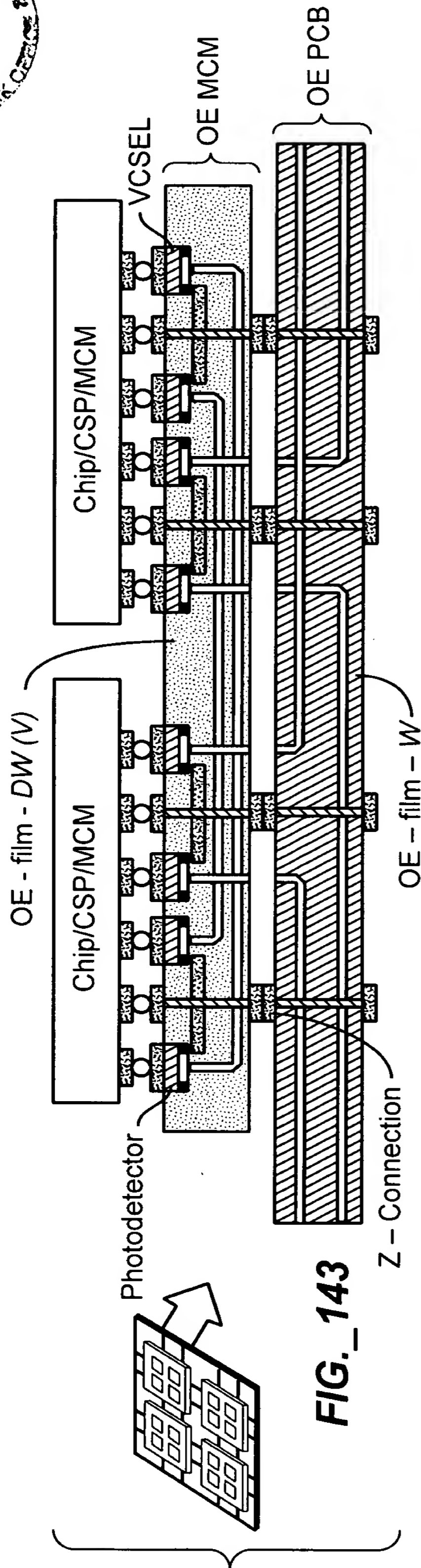


FIG. 143

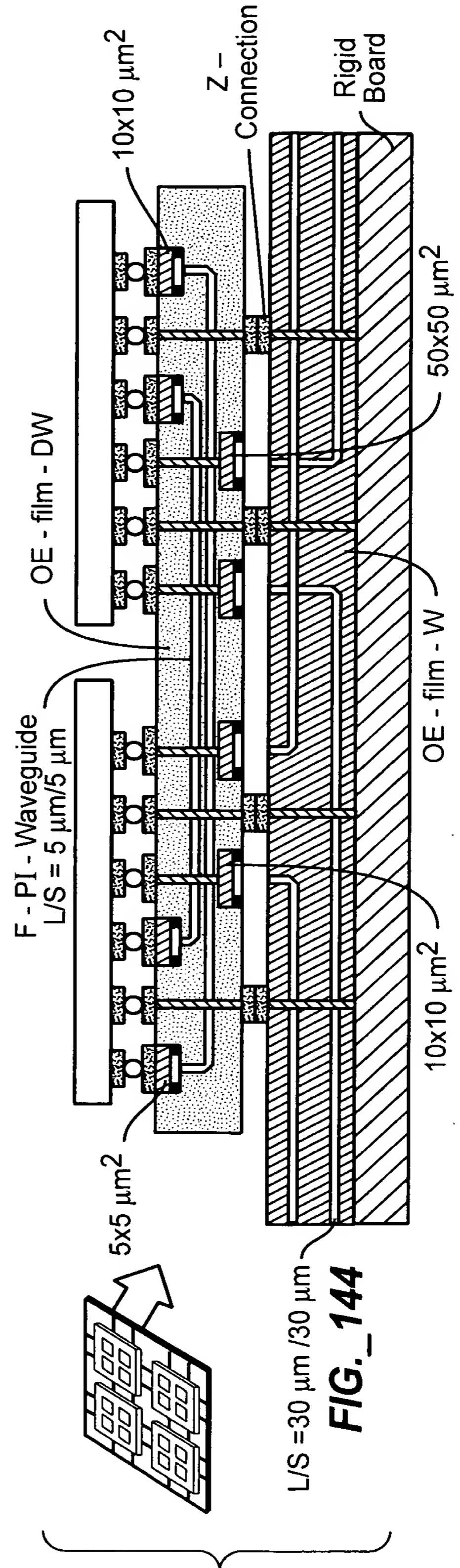
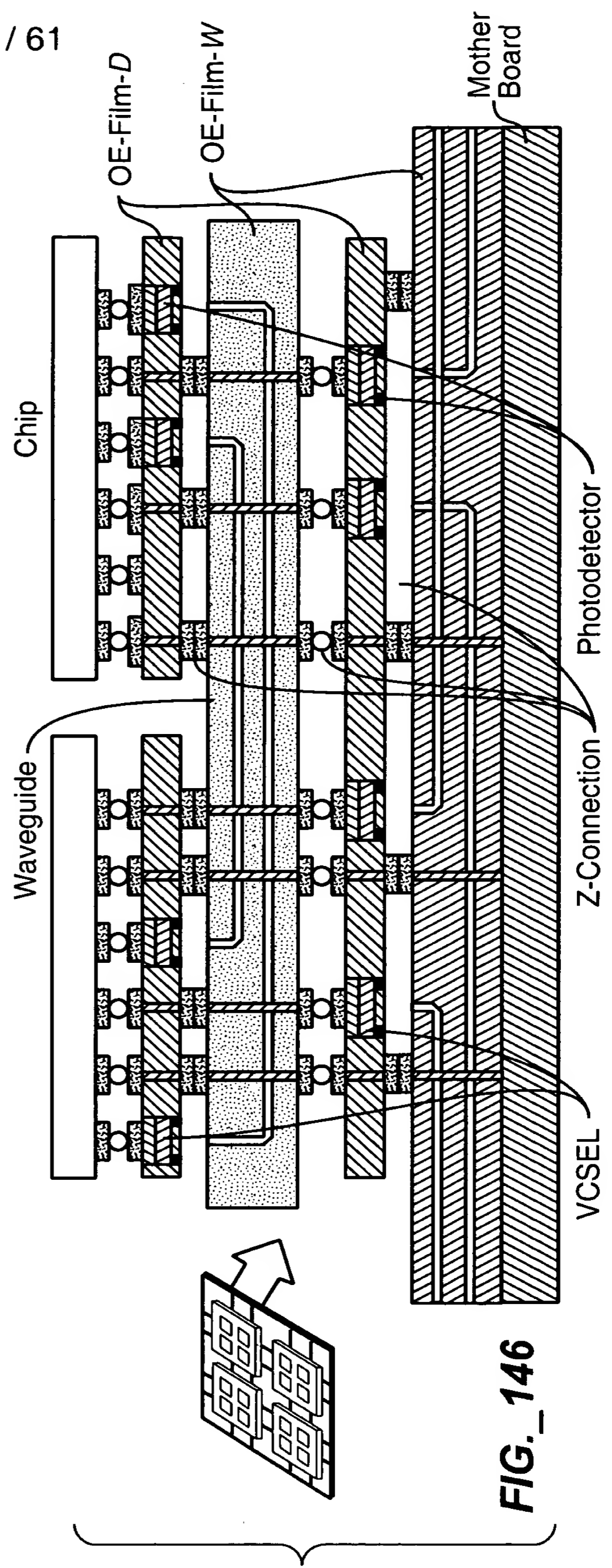
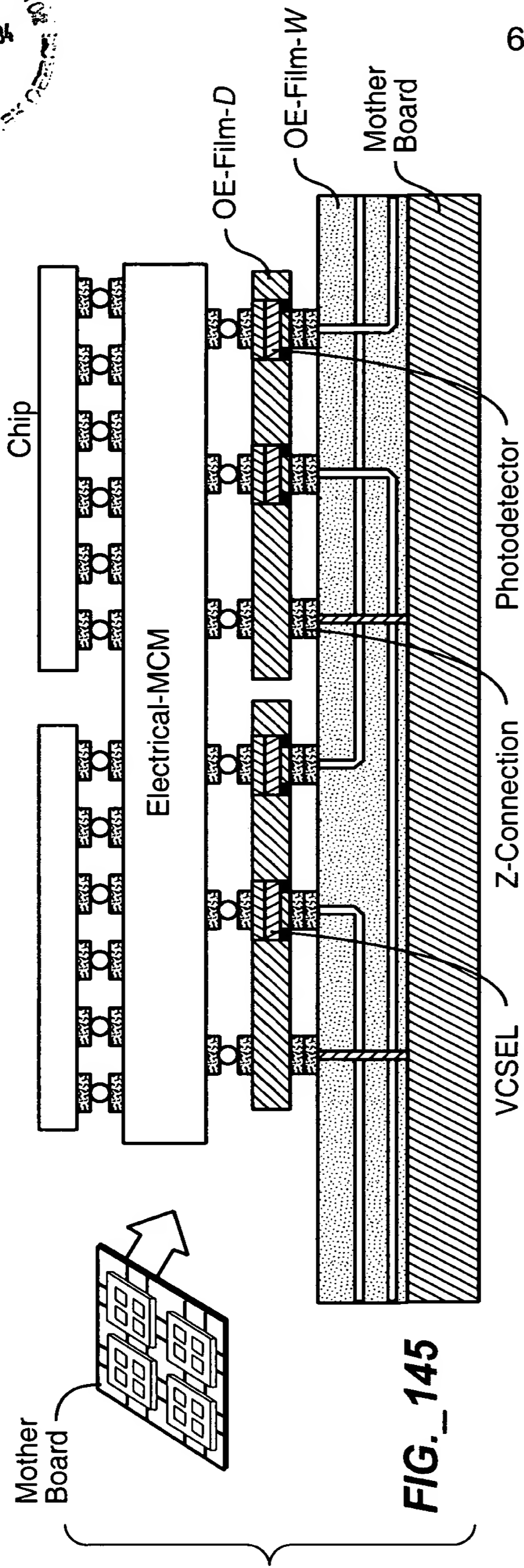


FIG. 144



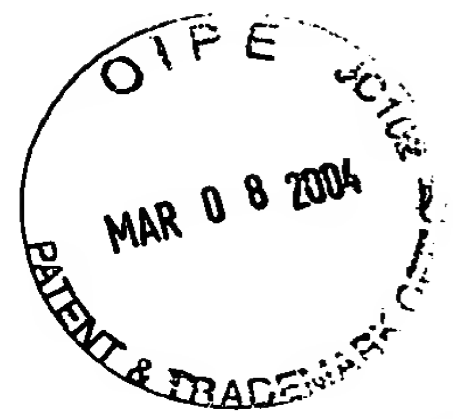


FIG._147

(PADS/LINES FORMATION)

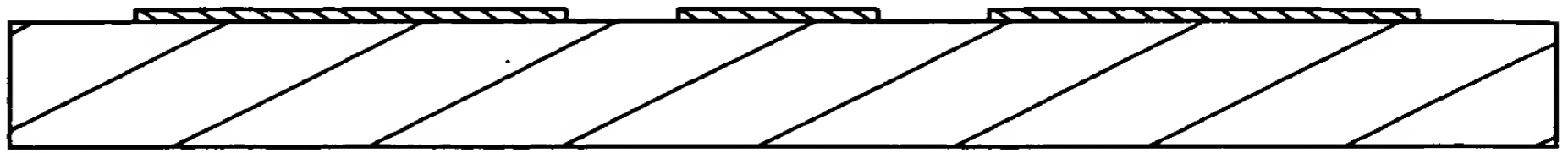


FIG._148

(PLACEMENT OF THIN-FILM DEVICES)

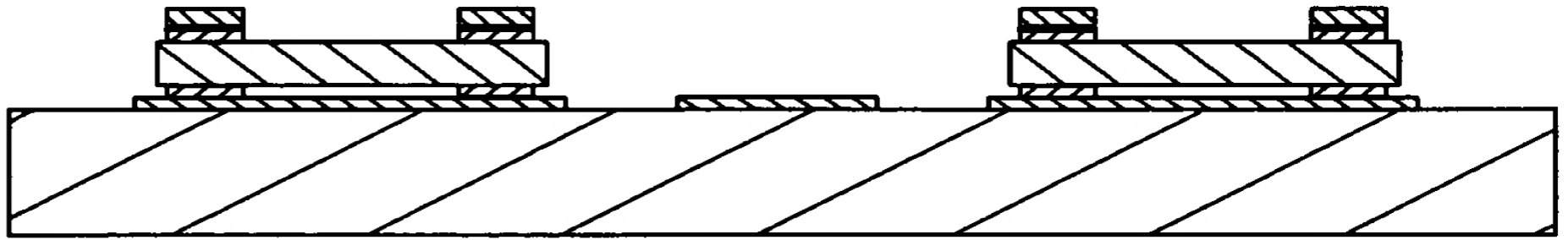


FIG._149

(POLYMER COAT)

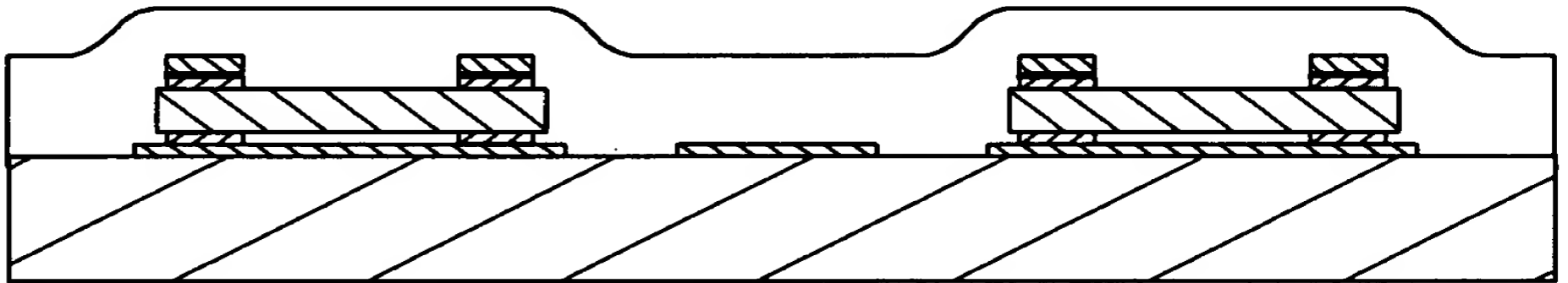


FIG._150

(PLANARIZATION)

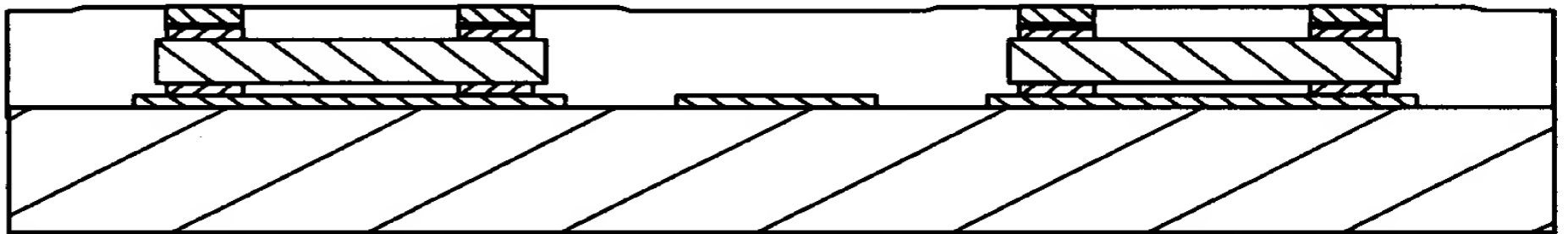


FIG._151

(VIAS/PADS/LINES FORMATION)

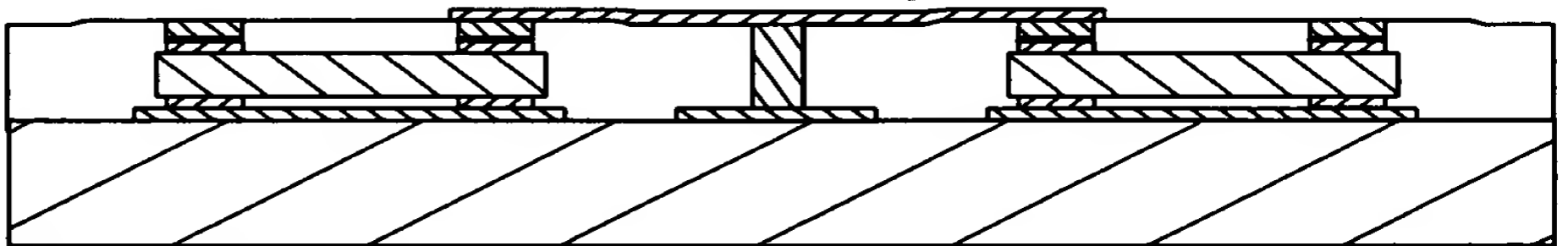


FIG._152

(SUBSTRATE REMOVAL)



FIG._153

(WAVEGUIDE
FORMATION)

